# CKS32F103x8
# CKS32F103xB
## Mainstream 32-bit MCU with 64 or 128 KB Flash

## Features

**■Core: M3 core**

- Up to 72 MHz operating frequency, 1.25 DMIPS/MHz (Dhrystone 2.1) at 0 wait-state memory access
- Single-cycle multiplication and hardware division

**■Memories**

- 64 KB or 128 KB program Flash
- 20KB SRAM

**■Clock, reset and supply management**

- 2.0 to 3.6 V application supply and I/Os
- POR/PDR, programmable voltage detector (PVD)
- 4 to 16 MHz crystal oscillator
- Internal factory-trimmed 8 MHz high-speed RC
- Internal 40 kHz low-speed RC with calibration
- PLL for CPU clock
- 32 kHz oscillator for RTC with calibration

**■2 × 12-bit, 1 µs A/D converters (up to 16 input channels)**

- Conversion range: 0 to 3.6 V
- Dual sample and hold capability
- Temperature sensor

**■DMA:**

- 7-channel DMA controller
- Peripherals supported: timers, ADC, SPI, $I^2C$ and USART

**■Low power**

- Sleep, Stop and Standby modes
- $V_{BAT}$ supply for RTC and backup registers



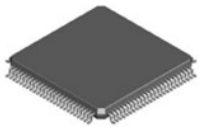
QFN36 6 x 6 mm



LQFP48 7 x 7 mm



LQFP64 10 x 10 mm



LQFP100 14 x 14 mm

**■Up to 80 fast I/O ports**

- 26/37/51/80 I/Os, all mappable on 16 external interrupt vectors; almost all 5 V-tolerant

**■Debug mode**

- Serial wire debug (SWD) and JTAG interfaces

**■7 timers**

- Three 16-bit timers, each with up to 4 IC/OC/PWM or pulse counter channels and quadrature (incremental) encoder input
- One 16-bit, motor-control PWM advanced-control timer with dead-time generation and emergency stop
- 2 watchdog timers (independent and window)
- SysTick timer: 24-bit down-counter

**■Up to 9 communication interfaces**

- Up to 2 × $I^2C$ interfaces (SMBus/PMBus)
- Up to 3 USARTs (ISO7816 interface, LIN, IrDA capability, modem control)
- Up to 2 SPIs (18 Mbit/s)
- CAN interface (2.0B Active)
- USB 2.0 full-speed interface

**■CRC calculation unit, 96-bit unique ID**

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# Device Comparison

**CKS32F103x8(B) features and peripheral counts**

| Part number / Peripherals | | CKS32F103T8/TB | | CKS32F103C8/CB | | CKS32F103R8/RB | | CKS32F103VB |
|---|---|---|---|---|---|---|---|---|
| Flash - Kbytes | | 64 | 128 | 64 | 128 | 64 | 128 | 128 |
| SRAM - Kbytes | | 20 | | 20 | | 20 | | 20 |
| Timers | General-purpose | 3 | | 3 | | 3 | | 3 |
| | Advanced-control | 1 | | 1 | | 1 | | 1 |
| Communication interfaces | SPI | 1 | | 2 | | 2 | | 2 |
| | I2C | 1 | | 2 | | 2 | | 2 |
| | USART | 2 | | 3 | | 3 | | 3 |
| | USB | 1 | | 1 | | 1 | | 1 |
| | CAN | 1 | | 1 | | 1 | | 1 |
| GPIOs (channels) | | 26 | | 37 | | 51 | | 80 |
| 12-bit synchronized ADC (channels) | | 2<br>10 channels | | 2<br>10 channels | | 2<br>16 channels | | 2<br>16 channels |
| CPU frequency | | 72 MHz | | | | | | |
| Operating voltage | | 2.0V ~3.6V | | | | | | |
| Operating temperature | | Ambient temperature: -40°C to ＋85°C (suffix 6) / -40°C to ＋105°C (suffix 7)<br>Junction temperature: -40°C to ＋125°C | | | | | | |
| Package | | QFN36 | | LQFP48/QFN48 | | LQFP64 | | LQFP100 |

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# Ordering Information

Tray packing

| Part number | Package | Qty/tray | Trays/box | Qty/box | Boxes/carton | Qty/carton |
|---|---|---|---|---|---|---|
| CKS32F103T8U6 | QFN36 | 490 PCS/tray | 10 trays/box | 4900 PCS/box | 6 boxes/carton | 29400 PCS/carton |
| CKS32F103TBU6 | QFN36 | 490 PCS/tray | 10 trays/box | 4900 PCS/box | 6 boxes/carton | 29400 PCS/carton |
| CKS32F103C8T6 | LQFP48 | 250 PCS/tray | 10 trays/box | 2500 PCS/box | 6 boxes/carton | 15000 PCS/carton |
| CKS32F103CBT6 | LQFP48 | 250 PCS/tray | 10 trays/box | 2500 PCS/box | 6 boxes/carton | 15000 PCS/carton |
| CKS32F103CBU6 | QFN48 | 260 PCS/tray | 10 trays/box | 2600 PCS/box | 6 boxes/carton | 15600 PCS/carton |
| CKS32F103R8T6 | LQFP64 | 160 PCS/tray | 10 trays/box | 1600 PCS/box | 6 boxes/carton | 9600 PCS/carton |
| CKS32F103RBT6/7 | LQFP64 | 160 PCS/tray | 10 trays/box | 1600 PCS/box | 6 boxes/carton | 9600 PCS/carton |
| CKS32F103VBT6 | LQFP100 | 90 PCS/tray | 10 trays/box | 900 PCS/box | 6 boxes/carton | 5400 PCS/carton |

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# 1. Introduction

This document gives the device characteristics of the CKS CKS32F103x8 and CKS32F103xB mainstream MCU products.

The CKS32F103x8 and CKS32F103xB datasheet must be read in conjunction with the related reference manual.

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# 2. Description

The CKS32F103x8 and CKS32F103xB mainstream MCU family incorporates the high-performance M3 32-bit RISC core operating at 72 MHz, high-speed embedded memories (Flash memory up to 128 Kbytes and SRAM of 20 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer two 12-bit ADCs, three general-purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two $I^2C$s and SPIs, three USARTs, one USB and one CAN.

The CKS32F103x8 and CKS32F103xB mainstream MCU family operates from a 2.0 V to 3.6 V power supply, over the -40°C to +85°C temperature range (suffix 6). A comprehensive set of power-saving modes allows the design of low-power applications.

The CKS32F103x8 and CKS32F103xB mainstream family includes devices in four different package types, from 36 pins to 100 pins. Depending on the package chosen, different sets of peripherals are included. The description below gives an overview of the complete range of peripherals proposed in this family.

These features make the CKS32F103x8 and CKS32F103xB mainstream microcontroller family suitable for a wide range of applications:

- Motor drives and application control
- Medical and handheld equipment
- PC and gaming peripherals and GPS platforms
- Industrial applications: PLCs, inverters, printers and scanners
- Alarm systems, video intercom, and HVAC systems, etc.

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## 2.1 Overview

### 2.1.1 M3 core with embedded Flash and SRAM

The M3 processor is the latest-generation embedded processor. It provides a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low system power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The M3 is a 32-bit RISC processor that offers superior code efficiency, delivering the high performance expected of a 32-bit core in the memory size usually associated with 8- and 16-bit devices.

With its embedded 32-bit core, the CKS32F103x8 and CKS32F103xB mainstream family is compatible with all 32-bit tools and software. Figure 1 shows the functional block diagram of the family.

### 2.1.2 Embedded Flash memory

64 or 128 Kbytes of embedded Flash memory is available for storing programs and data.

### 2.1.3 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link time and stored at a given memory location.

### 2.1.4 Embedded SRAM

20 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

### 2.1.5 Nested vectored interrupt controller (NVIC)

The CKS32F103x8 and CKS32F103xB mainstream devices embed a nested vectored interrupt controller able to handle up to 43 maskable interrupt channels (not including the 16 interrupt lines of M3) and 16 priority levels.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late-arriving higher-priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt return with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

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### 2.1.6 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal APB2 clock period. Up to 80 GPIOs are connected to the 16 external interrupt lines.

### 2.1.7 Clocks and startup

System clock selection is performed on startup. The internal 8 MHz RC oscillator is selected as the default CPU clock on reset. An external 4-16 MHz clock can then be selected, which is monitored for failure. If a failure is detected, the external clock is isolated and the system automatically switches back to the internal RC oscillator; a software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example, when an indirectly used external oscillator fails).

Several prescalers allow the configuration of the AHB frequency, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the AHB and high-speed APB domains is 72 MHz; the maximum allowed frequency of the low-speed APB domain is 36 MHz. See the clock tree diagram in Figure 2.

### 2.1.8 Boot modes

At startup, the boot pins are used to select one of three boot options:

- Boot from program Flash memory
- Boot from system memory
- Boot from embedded SRAM

The bootloader is located in system memory. It is used to reprogram the Flash memory via USART1.

### 2.1.9 Power supply schemes

- $V_{DD}$ = 2.0 to 3.6 V: external power supply for the I/Os and the internal regulator, provided through the $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supply for the ADC, reset blocks, RC oscillators and PLL. $V_{DDA}$ must be at least 2.4 V when the ADC is used. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ = 1.8 to 3.6 V: power supply for the RTC, external 32 kHz oscillator and backup registers (through an internal power switch) when $V_{DD}$ is not present.

For more details on how to connect the power pins, refer to the Power supply scheme figure.

### 2.1.10 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active and ensures proper operation starting from/down to 2 V. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit. The device also features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}$ drops below or rises above the $V_{PVD}$ threshold; the interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

Refer to Table 8 for the values of $V_{POR/PDR}$ and $V_{PVD}$.

### 2.1.11 Voltage regulator

The regulator has three operating modes: main (MR), low-power (LPR) and power-down

- MR is used in normal (Run) operating mode
- LPR is used in the Stop mode of the CPU
- Power-down is used in Standby mode of the CPU: the regulator output is in high impedance, the kernel circuitry is powered down, and the regulator draws zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing a high-impedance output.

### 2.1.12 Low-power modes

The CKS32F103x8 and CKS32F103xB mainstream devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources.

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- Sleep mode

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Stop mode

Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. In Stop mode, all clocks in the 1.5 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled, and the voltage regulator can be put in either normal or low-power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external I/O lines, the PVD output, the RTC alarm or the USB wakeup.

- Standby mode

Standby mode achieves the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.5 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost, except for the backup registers and the standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG and the corresponding clock sources are not stopped by entering Stop or Standby mode.

### 2.1.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management, avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software, and the transfer size, source and destination addresses are independently programmable.

The DMA can be used with the main peripherals: SPI, $I^2C$, USART, general-purpose, basic and advanced-control timers TIMx, and ADC.

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### 2.1.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power from either the $V_{DD}$ supply when present or the $V_{BAT}$ pin. The backup registers (ten 16-bit registers) can be used to store 20 bytes of user application data when $V_{DD}$ power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock-calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator, or the high-speed external clock divided by 128. The internal low-power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long-term measurement using the compare register. A 20-bit prescaler is used for the time-base clock and is by default configured to generate a time base of 1 second from a 32.768 kHz clock.

### 2.1.15 Timers and watchdogs

The CKS32F103x8 and CKS32F103xB mainstream devices include one advanced-control timer, three general-purpose timers, two watchdog timers and one SysTick timer.

The table below compares the features of the advanced-control, general-purpose and basic timers:

Table 1 Timer feature comparison

| Timers | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|
| TIM1 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | Yes |
| TIM2<br>TIM3<br>TIM4 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |

#### Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM generator multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

When configured as a standard 16-bit timer, it has the same features as the TIMx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the counter can be frozen and the PWM outputs disabled, so as to turn off any power switches driven by these outputs.

Many features are shared with those of the standard TIM timers, which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

#### General-purpose timers (TIMx)

There are up to 3 synchronizable standard timers (TIM2, TIM3 and TIM4) embedded in the CKS32F103x8 and CKS32F103xB mainstream devices. Each timer features a 16-bit auto-reload up/down counter, a 16-bit prescaler and 4 independent channels, each of which can be used for input capture, output compare, PWM or one-pulse mode output. This gives up to 12 input capture/output compare/PWM channels on the largest packages.

They can work together with the advanced-control timer via the Timer Link feature for synchronization or event chaining. Their counters can be frozen in debug mode. Any of the standard timers can be used to generate PWM outputs. Each timer has independent DMA request generation.

These timers are also capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 Hall-effect sensors.

#### Independent watchdog

The independent watchdog is based on a 12-bit down-counter and an 8-bit prescaler. It is clocked from an independent 40 kHz internal RC; as it operates independently of the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes. The counter can be frozen in debug mode.

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Window watchdog

The window watchdog is based on a 7-bit down-counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock and has an early warning interrupt capability; the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but can also be used as a standard down-counter. It features:

- A 24-bit down-counter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

### 2.1.16 I2C bus

Up to two $I^2C$ bus interfaces can operate in multimaster and slave modes. They support standard and fast modes.

The $I^2C$ interfaces support 7-bit or 10-bit addressing, and 7-bit dual addressing in slave mode. A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

### 2.1.17 Universal synchronous/asynchronous receiver transmitter (USART)

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s; the other interfaces communicate at up to 2.25 Mbit/s. The USART interfaces provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO7816 smartcard compliant and have LIN master/slave capability.

All USART interfaces can be served by the DMA controller.

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### 2.1.18 Serial peripheral interface (SPI)

Up to two SPIs are able to communicate at up to 18 Mbit/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies, and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

### 2.1.19 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and 2.0B (active) with a bit rate of up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages, and 14 scalable filter banks.

### 2.1.20 Universal serial bus (USB)

The CKS32F103x8 and CKS32F103xB mainstream devices embed a USB device peripheral compatible with USB full speed,

conforming to the USB full-speed device (12 Mbit/s) standard, with software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz USB clock is generated directly from the internal main PLL (the clock source must be an HSE crystal oscillator).

### 2.1.21 General-purpose inputs/outputs (GPIOs)

Each GPIO pin can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down, floating) or as peripheral alternate function. Most GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable except for analog inputs.

The I/O alternate function configuration can be locked if needed following a specific sequence, in order to avoid spurious writing to the I/O registers. I/Os on APB2 have a toggling speed of up to 18 MHz.

### 2.1.22 ADC (analog-to-digital converter)

The CKS32F103x8 and CKS32F103xB mainstream devices embed two 12-bit analog-to-digital converters (ADCs), sharing up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the monitored signal is outside the programmed thresholds.

The events generated by the standard timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger and injection trigger respectively, allowing the application to synchronize A/D conversion and timers.

### 2.1.23 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The conversion range is $2\ V < V_{DDA} < 3.6\ V$. The temperature sensor is internally connected to the ADC12_IN16 input channel, which is used to convert the sensor output voltage into a digital value.

### 2.1.24 Serial wire JTAG debug port (SWJ-DP)

An embedded SWJ-DP interface combines a JTAG and a serial wire debug port, enabling either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

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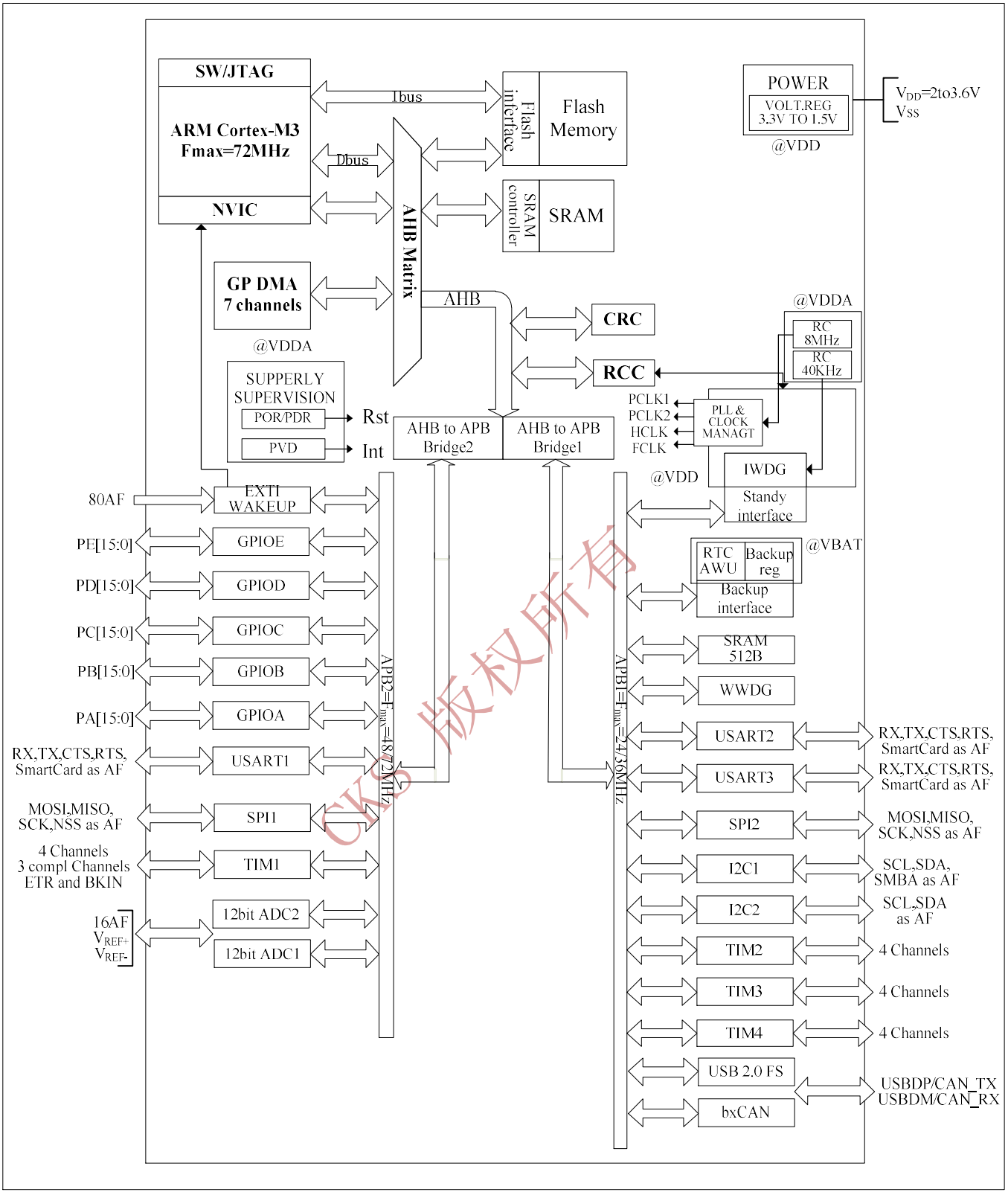


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Figure 1 System block diagram

1. Operating temperature: -40°C to +85°C, junction temperature up to 105°C.
2. AF: I/O port usable as a peripheral alternate-function pin

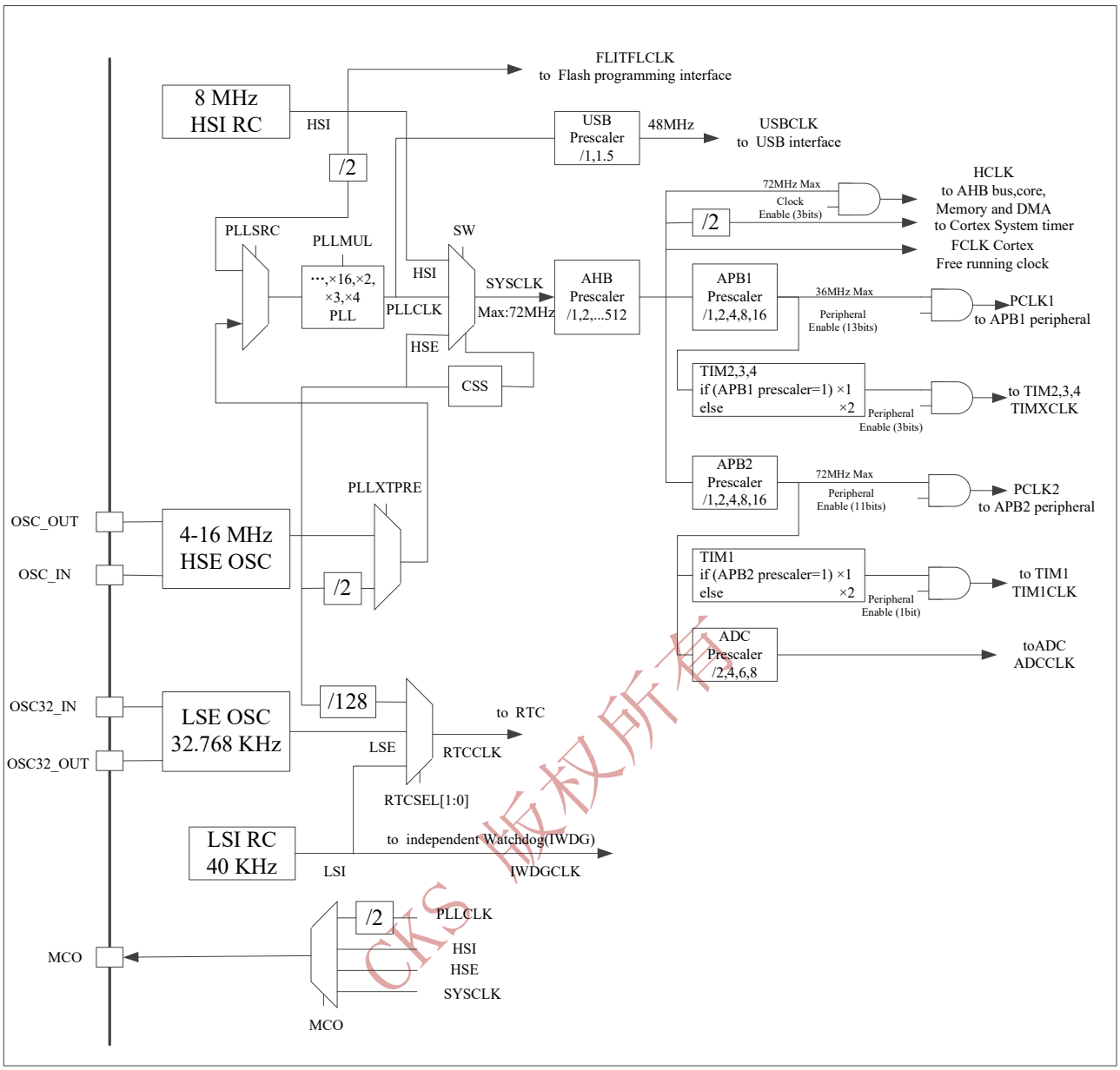


Figure 2 Clock tree

1. When HSI is used as the PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. When the USB function is used, both HSE and PLL must be used, and the CPU must run at 48 MHz or 72 MHz.
3. To obtain an ADC sampling time of 1 µs, APB2 must be set to 14 MHz, 28 MHz or 56 MHz.

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# 3. Pinouts and Pin Description

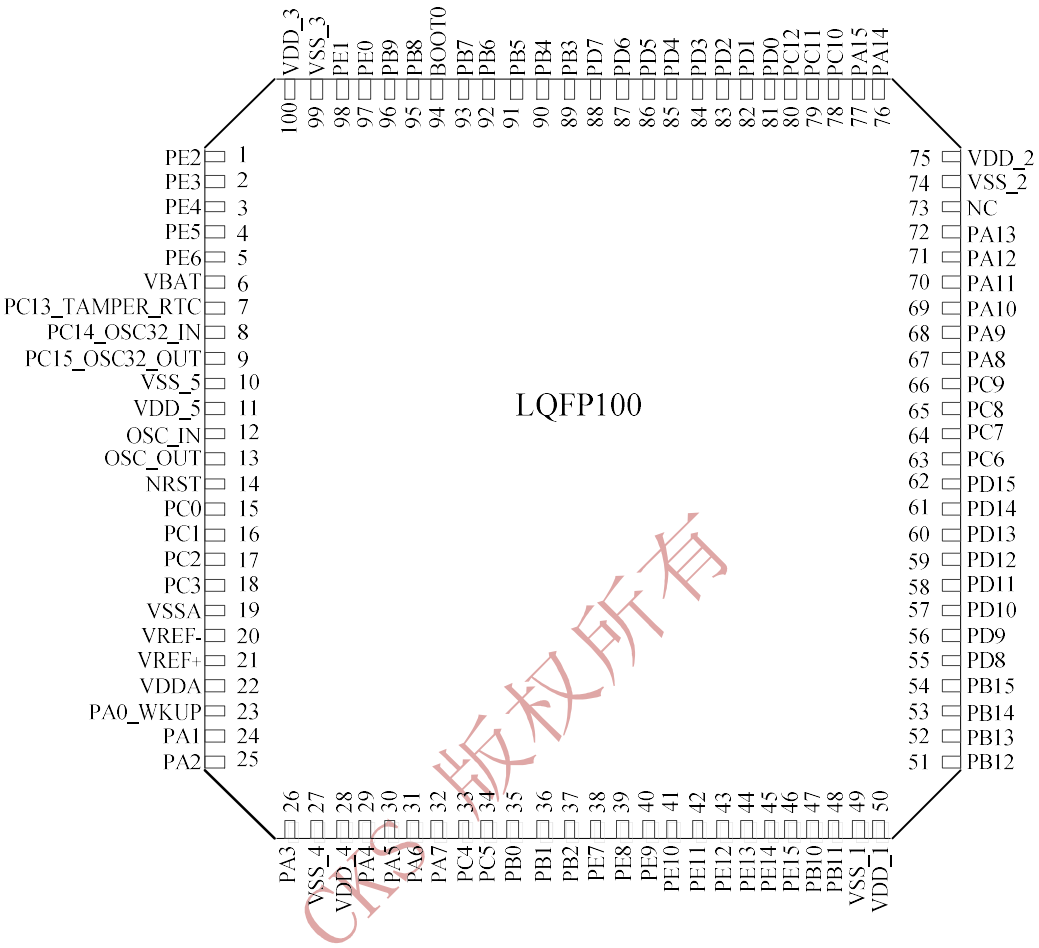


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Figure 3 CKS32F103xx mainstream LQFP100 pinout

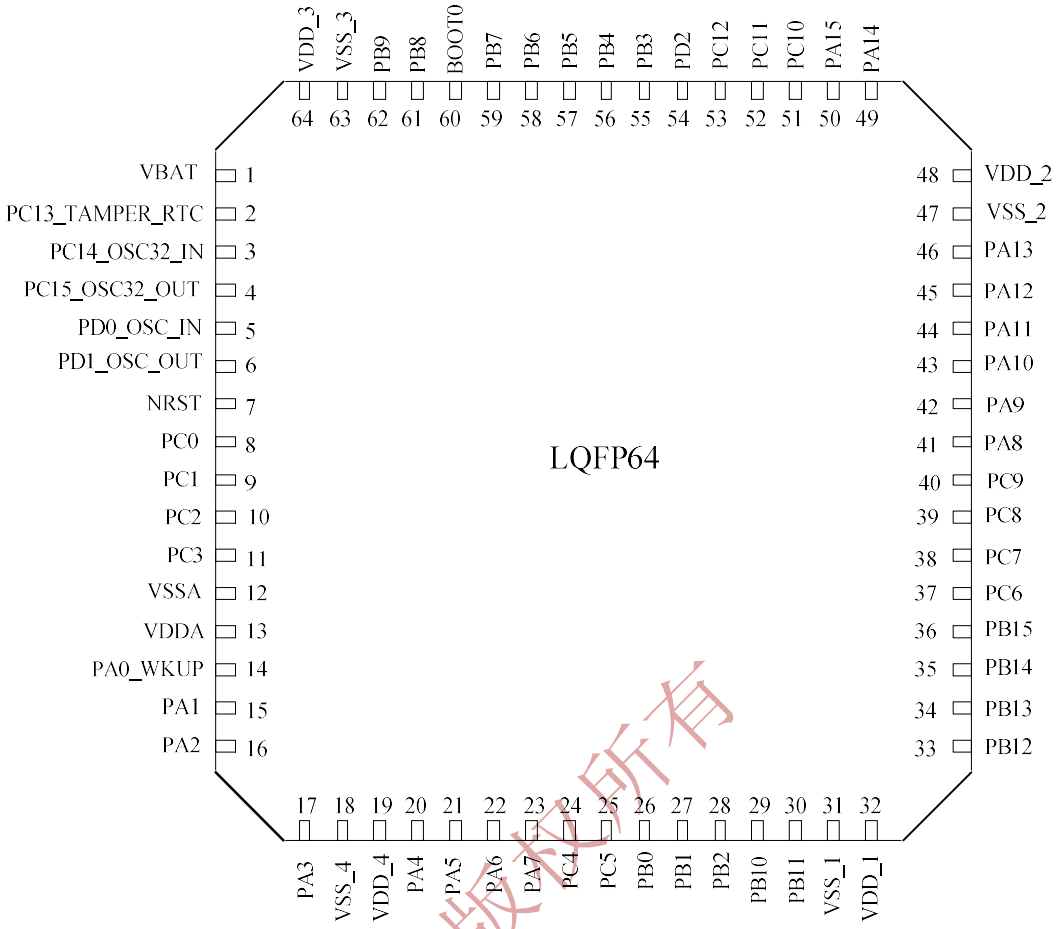


Figure 4 CKS32F103xx mainstream LQFP64 pinout

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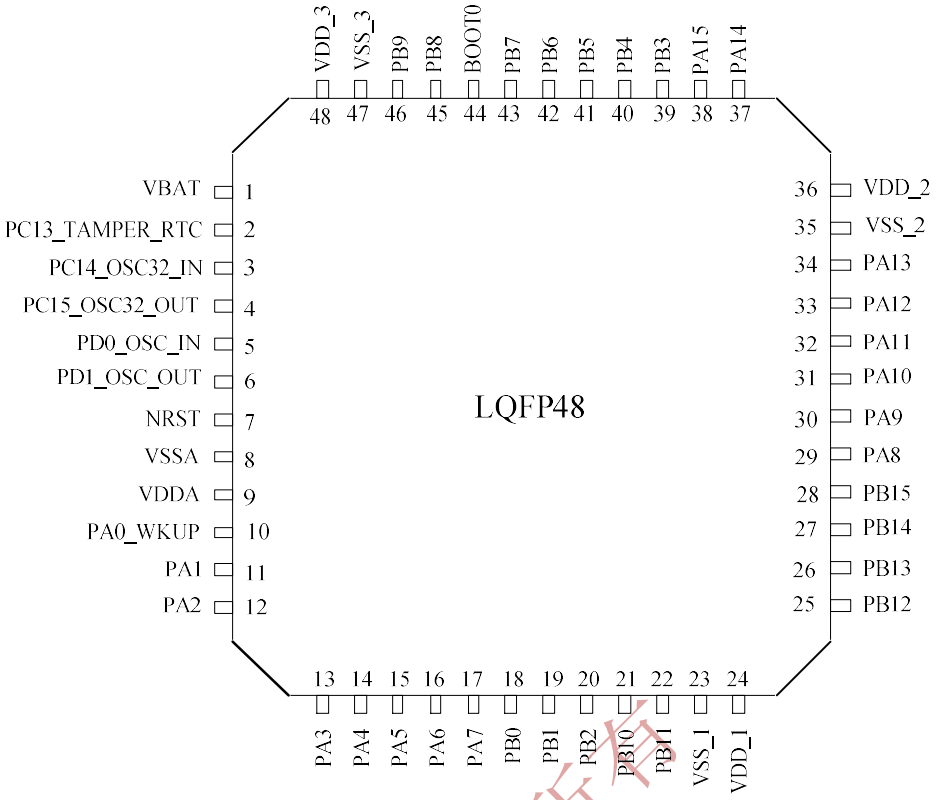


Figure 5 CKS32F103xx mainstream LQFP48 pinout

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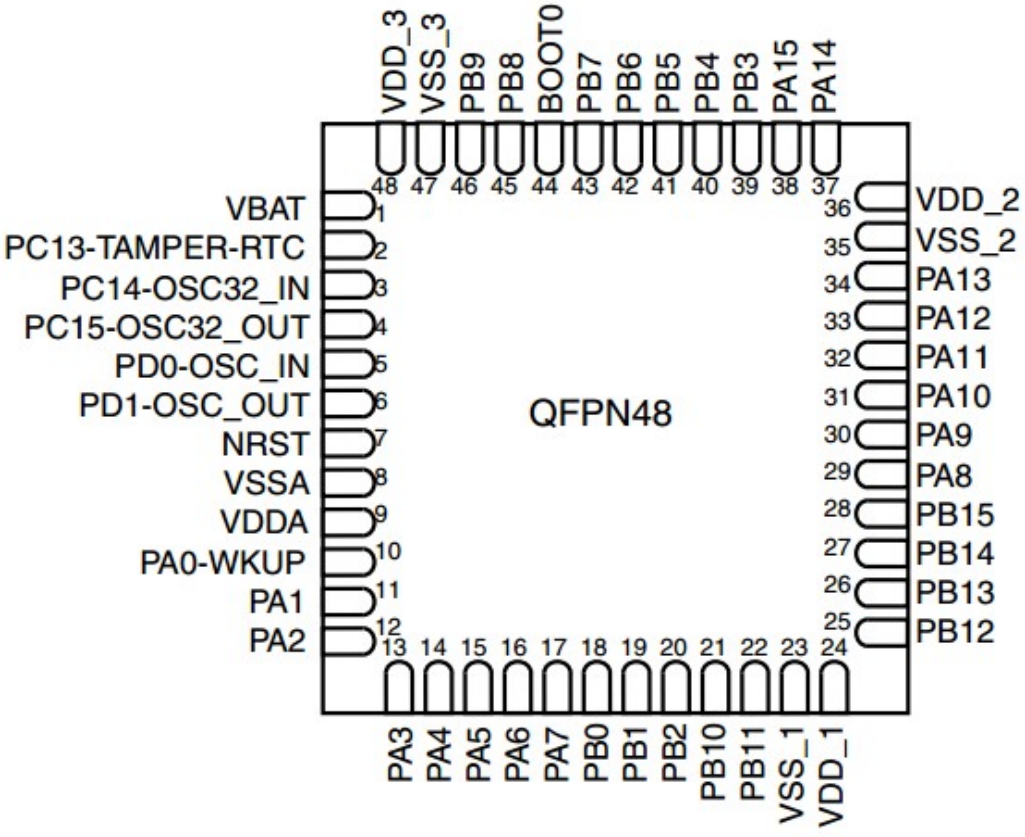


Figure 6 CKS32F103xx mainstream QFPN48 pinout

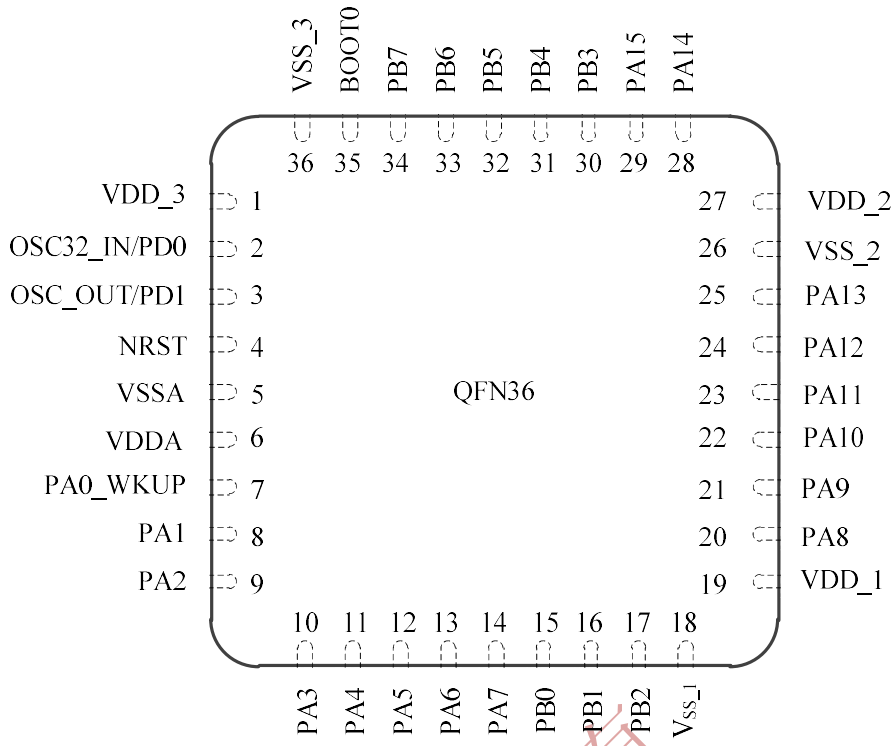


Figure 7 CKS32F103xx mainstream QFN36 pinout

Table 2 CKS32F103xx pin definitions

| Pin number | | | | | Pin name | Type (1) | I/O level (2) | Main function(3) (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | LQFP100 | QFN48 | QFN36 | | | | | | |
| - | - | 1 | - | - | PE2 | I/O | FT | PE2 | TRACECK | |
| - | - | 2 | - | - | PE3 | I/O | FT | PE3 | TRACED0 | |
| - | - | 3 | - | - | PE4 | I/O | FT | PE4 | TRACED1 | |
| - | - | 4 | - | - | PE5 | I/O | FT | PE5 | TRACED2 | |
| - | - | 5 | - | - | PE6 | I/O | FT | PE6 | TRACED3 | |
| 1 | 1 | 6 | 1 | - | $V_{BAT}$ | S | | $V_{BAT}$ | | |
| 2 | 2 | 7 | 2 | - | PC13-TAMPER-RTC(4) | I/O | | PC13 | TAMPER-RTC | |
| 3 | 3 | 8 | 3 | - | PC14-OSC32_IN(4) | I/O | | PC14 | OSC32_IN | |
| 4 | 4 | 9 | 4 | - | PC15-OSC32_OUT(4) | I/O | | PC15 | OSC32_OUT | |
| - | - | 10 | - | - | $V_{SS_5}$ | S | | $V_{SS_5}$ | | |
| - | - | 11 | - | - | $V_{DD_5}$ | S | | $V_{DD_5}$ | | |
| 5 | 5 | 12 | 5 | 2 | OSC_IN | I | | OCS_IN | | PD0(7) |

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| Pin number | | | | | Pin name | Type (1) | I/O I/O level (2) | Main function(3) (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | LQFP100 | QFN48 | QFN36 | | | | | | |
| 6 | 6 | 13 | 6 | 3 | OSC_OUT | O | | OSC_OUT | | PD1(7) |
| 7 | 7 | 14 | 7 | 4 | NRST | I/O | | NRST | | |
| - | 8 | 15 | - | - | PC0 | I/O | | PC0 | ADC12_IN10 | |
| - | 9 | 16 | - | - | PC1 | I/O | | PC1 | ADC12_IN11 | |
| - | 10 | 17 | - | - | PC2 | I/O | | PC2 | ADC12_IN12 | |
| - | 11 | 18 | - | - | PC3 | I/O | | PC3 | ADC12_IN13 | |
| 8 | 12 | 19 | 8 | 5 | $V_{SSA}$ | S | | $V_{SSA}$ | | |
| - | - | 20 | - | - | $V_{REF-}$ | S | | $V_{REF-}$ | | |
| - | - | 21 | - | - | $V_{REF+}$ | S | | $V_{REF+}$ | | |
| 9 | 13 | 22 | 9 | 6 | $V_{DDA}$ | S | | $V_{DDA}$ | | |
| 10 | 14 | 23 | 10 | 7 | PA0-WKUP | I/O | | PA0 | WKUP/USART2_CTS(6)/ADC12_IN0/ TIM2_CH1_ETR(6) | |
| 11 | 15 | 24 | 11 | 8 | PA1 | I/O | | PA1 | USART2_RTS(6)/ ADC12_IN1/ TIM2_CH2(6) | |
| 12 | 16 | 25 | 12 | 9 | PA2 | I/O | | PA2 | USART2_TX(6)/ADC12_IN2/TIM2_CH3(6) | |
| 13 | 17 | 26 | 13 | 10 | PA3 | I/O | | PA3 | USART2_RX(6)/ADC12_IN3/TIM2_CH4(6) | |
| - | 18 | 27 | - | - | $V_{SS_4}$ | S | | $V_{SS_4}$ | | |
| - | 19 | 28 | - | - | $V_{DD_4}$ | S | | $V_{DD_4}$ | | |
| 14 | 20 | 29 | 14 | 11 | PA4 | I/O | | PA4 | SPI1_NSS(6)/ USART2_CK(6)/ ADC12_IN4 | |
| 15 | 21 | 30 | 15 | 12 | PA5 | I/O | | PA5 | SPI1_SCK(6)/ ADC12_IN5 | |
| 16 | 22 | 31 | 16 | 13 | PA6 | I/O | | PA6 | SPI1_MISO(6)/ ADC12_IN6/ TIM3_CH1(6) | TIM1_BKIN |
| 17 | 23 | 32 | 17 | 14 | PA7 | I/O | | PA7 | SPI1_MOSI(6)/ ADC12_IN7/ TIM3_CH2(6) | TIMI_CHIN |
| - | 24 | 33 | - | - | PC4 | I/O | | PC4 | ADC12_IN14 | |
| - | 25 | 34 | - | - | PC5 | I/O | | PC5 | ADC12_IN15 | |
| 18 | 26 | 35 | 18 | 15 | PB0 | I/O | | PB0 | ADC12_IN8/ | TIM1_CH2N |

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| Pin number | | | | | Pin name | Type (1) | I/O I/O level (2) | Main function(3) (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | LQFP100 | QFN48 | QFN36 | | | | | | |
| | | | | | | | | | TIM3_CH3(6) | |
| 19 | 27 | 36 | 19 | 16 | PB1 | I/O | | PB1 | ADC12_IN9/ TIM3_CH4(6) | TIM1_CH3N |
| 20 | 28 | 37 | 20 | 17 | PB2 | I/O | FT | PB2/ BOOT1 | | |
| - | - | 38 | - | - | PE7 | I/O | FT | PE7 | | TIM1_ETR |
| - | - | 39 | - | - | PE8 | I/O | FT | PE8 | | TIM1_CH1N |
| - | - | 40 | - | - | PE9 | I/O | FT | PE9 | | TIM1_CH1 |
| - | - | 41 | - | - | PE10 | I/O | FT | PE10 | | TIM1_CH2N |
| - | - | 42 | - | - | PE11 | I/O | FT | PE11 | | TIM1_CH2 |
| - | - | 43 | - | - | PE12 | I/O | FT | PE12 | | TIM1_CH3N |
| - | - | 44 | - | - | PE13 | I/O | FT | PE13 | | TIM1_CH3 |
| - | - | 45 | - | - | PE14 | I/O | FT | PE14 | | TIM1_CH4 |
| - | - | 46 | - | - | PE15 | I/O | FT | PE15 | | TIM1_BKIN |
| 21 | 29 | 47 | 21 | - | PB10 | I/O | FT | PB10 | I2C2_SCL/ USART3_TX(6) | TIM2_CH3 |
| 22 | 30 | 48 | 22 | - | PB11 | I/O | FT | PB11 | I2C2_SDA/ USART3_RX(6) | TIM2_CH4 |
| 23 | 31 | 49 | 23 | 18 | $V_{SS_1}$ | S | | $V_{SS_1}$ | | |
| 24 | 32 | 50 | 24 | 19 | $V_{DD_1}$ | S | | $V_{DD_1}$ | | |
| 25 | 33 | 51 | 25 | - | PB12 | I/O | FT | PB12 | SPI2_NSS/ I2C2_SMBAI/ USART3_CK(6)/ TIM1_BKIN(6) | |
| 26 | 34 | 52 | 26 | - | PB13 | I/O | FT | PB13 | SPI2_SCK/ USART3_CTS(6)/ TIM1_CH1N(6) | |
| 27 | 35 | 53 | 27 | - | PB14 | I/O | FT | PB14 | SPI2_MISO/ USART3_RTS(6)/ TIM1_CH2N(6) | |
| 28 | 36 | 54 | 28 | - | PB15 | I/O | FT | PB15 | SPI2_MOSI/ TIM1_CH3N(6) | |
| - | - | 55 | - | - | PD8 | I/O | FT | PD8 | | USART3_TX |
| - | - | 56 | - | - | PD9 | I/O | FT | PD9 | | USART3_RX |
| - | - | 57 | - | - | PD10 | I/O | FT | PD10 | | USART3_CK |
| - | - | 58 | - | - | PD11 | I/O | FT | PD11 | | USART3_CTS |
| - | - | 59 | - | - | PD12 | I/O | FT | PD12 | | TIM4_CH1/ USART3_RTS |

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| Pin number | | | | | Pin name | Type (1) | I/O level (2) | Main function(3) (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | LQFP100 | QFN48 | QFN36 | | | | | | |
| - | - | 60 | - | - | PD13 | I/O | FT | PD13 | | TIM4_CH2 |
| - | - | 61 | - | - | PD14 | I/O | FT | PD14 | | TIM4_CH3 |
| - | - | 62 | - | - | PD15 | I/O | FT | PD15 | | TIM4_CH4 |
| - | 37 | 63 | - | - | PC6 | I/O | FT | PC6 | | TIM3_CH1 |
| - | 38 | 64 | - | - | PC7 | I/O | FT | PC7 | | TIM3_CH2 |
| - | 39 | 65 | - | - | PC8 | I/O | FT | PC8 | | TIM3_CH3 |
| - | 40 | 66 | - | - | PC9 | I/O | FT | PC9 | | TIM3_CH4 |
| 29 | 41 | 67 | 29 | 20 | PA8 | I/O | FT | PA8 | USART1_CK/ TIM1_CH1(6)/MCO | |
| 30 | 42 | 68 | 30 | 21 | PA9 | I/O | FT | PA9 | USART1_TX(6)/ TIM1_CH2(6) | |
| 31 | 43 | 69 | 31 | 22 | PA10 | I/O | FT | PA10 | USART1_RX(6)/ TIM1_CH3(6) | |
| 32 | 44 | 70 | 32 | 23 | PA11 | I/O | FT | PA11 | USART1_CTS/ USBDM/CANRX(6) /TIM1_CH4(6) | |
| 33 | 45 | 71 | 33 | 24 | PA12 | I/O | FT | PA12 | USART1_RTS/ USBDP/CANTX(6)/ TIM1_ETR(6) | |
| 34 | 46 | 72 | 34 | 25 | PA13 | I/O | FT | JTMS/SWD IO | | PA13 |
| - | - | 73 | - | - | Not connected | | | | | |
| 35 | 47 | 74 | 35 | 26 | $V_{SS_2}$ | S | | $V_{SS_2}$ | | |
| 36 | 48 | 75 | 36 | 27 | $V_{DD_2}$ | S | | $V_{DD_2}$ | | |
| 37 | 49 | 76 | 37 | 28 | PA14 | I/O | FT | JTCK/ SWCLK | | PA14 |
| 38 | 50 | 77 | 38 | 29 | PA15 | I/O | FT | JTDI | | TIM2_CH1_ETR PA15/SPI1_NSS |
| - | 51 | 78 | - | - | PC10 | I/O | FT | PC10 | | USART3_TX |
| - | 52 | 79 | - | - | PC11 | I/O | FT | PC11 | | USART3_RX |
| - | 53 | 80 | - | - | PC12 | I/O | FT | PC12 | | USART3_CK |
| | | 81 | | 2 | PD0 | I/O | FT | OSC_IN(8) | | CANRX |
| | | 82 | | 3 | PD1 | I/O | FT | OSC_OUT(8 ) | | CANTX |
| - | 54 | 83 | - | - | PD2 | I/O | FT | PD2 | TIM3_ETR | |
| - | - | 84 | - | - | PD3 | I/O | FT | PD3 | | USART2_CTS |
| - | - | 85 | - | - | PD4 | I/O | FT | PD4 | | USART2_RTS |
| - | - | 86 | - | - | PD5 | I/O | FT | PD5 | | USART2_TX |

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| Pin number | | | | | Pin name | Type (1) | I/O I/O level (2) | Main function(3) (after reset) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|---|
| LQFP48 | LQFP64 | LQFP100 | QFN48 | QFN36 | | | | | | |
| - | - | 87 | - | - | PD6 | I/O | FT | PD6 | | USART2_RX |
| - | - | 88 | - | - | PD7 | I/O | FT | PD7 | | USART2_CK |
| 39 | 55 | 89 | 39 | 30 | PB3 | I/O | FT | JTDO | | PB3/TRACESWO/ TIM2_CH2/ SPI1_SCK |
| 40 | 56 | 90 | 40 | 31 | PB4 | I/O | FT | JNTRST | | PB4/TIM3_CH1/ SPI1_MISO |
| 41 | 57 | 91 | 41 | 32 | PB5 | I/O | | PB5 | I2C1_SMBAI | TIM3_CH2/ SPI1_MOSI |
| 42 | 58 | 92 | 42 | 33 | PB6 | I/O | FT | PB6 | I2C1_SCL(6)/ TIM4_CH1(6) | USART1_TX |
| 43 | 59 | 93 | 43 | 34 | PB7 | I/O | FT | PB7 | I2C1_SDA(6)/ TIM4_CH2(6) | USART1_RX |
| 44 | 60 | 94 | 44 | 35 | BOOT0 | I | | BOOT0 | | |
| 45 | 61 | 95 | 45 | - | PB8 | I/O | FT | PB8 | TIM4_CH3(6) | I2C1_SCL/ CANRX |
| 46 | 62 | 96 | 46 | - | P89 | I/O | FT | P89 | TIM4_CH4(6) | I2C1_SDA/ CANTX |
| - | - | 97 | - | - | PE0 | I/O | FT | PE0 | TIM4_ETR | |
| - | - | 98 | - | - | PE1 | I/O | FT | PE1 | | |
| 47 | 63 | 99 | 47 | 36 | $V_{SS_3}$ | S | | $V_{SS_3}$ | | |
| 48 | 64 | 100 | 48 | 1 | $V_{DD_3}$ | S | | $V_{DD_3}$ | | |

1. I = input, O = output, S = supply
2. FT: 5 V tolerant
3. PC13, PC14 and PC15 are supplied through the power switch, which can sink only a limited amount of current (3 mA). Therefore the use of these three GPIOs in output mode is limited: they can be used only in 2 MHz output mode, with a maximum load of 30 pF, and must not be used as a current source (e.g. to drive an LED).
4. These pins are in main-function state on the first power-up of the backup domain. Afterwards, even after reset, their state is controlled by the backup domain registers (which are not reset by the main reset). For details on how to manage these I/Os, refer to the battery backup domain and BKP register sections of the CKS32F103x8 and CKS32F103xB reference manual.
5. This alternate function can be remapped by software to other pins (if available on the selected package). For details, refer to the alternate function I/O and debug configuration sections of the CKS32F103x8 and CKS32F103xB reference manual.
6. Pins 2 and 3 of the QFN36 package, and pins 5 and 6 of the LQFP48 and LQFP64 packages, are configured as OSC_IN/ OSC_OUT by default after reset. Software can reconfigure these two pins as PD0 and PD1. However, for the LQFP100 package, PD0 and PD1 are native function pins, so there is no need to remap them by software. For more details, refer to the alternate function I/O and debug configuration sections of the CKS32F103x8 and CKS32F103xB reference manual. In output mode, PD0 and PD1 can only be configured as 50 MHz outputs.
7. ADC12_INx (x is an integer from 0 to 15) appearing in the pin names of the table means this pin can be ADC1_INx or ADC2_INx. For

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example, ADC12_IN9 means this pin can be configured as either ADC1_IN9 or ADC2_IN9.

8. TIM2_CH1_ETR in the alternate functions of pin PA0 means the function can be configured as TIM2_TI1 or TIM2_ETR. Likewise, the remapped alternate function TIM2_CH1_ETR of PA15 has the same meaning.

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# 4. Memory Mapping

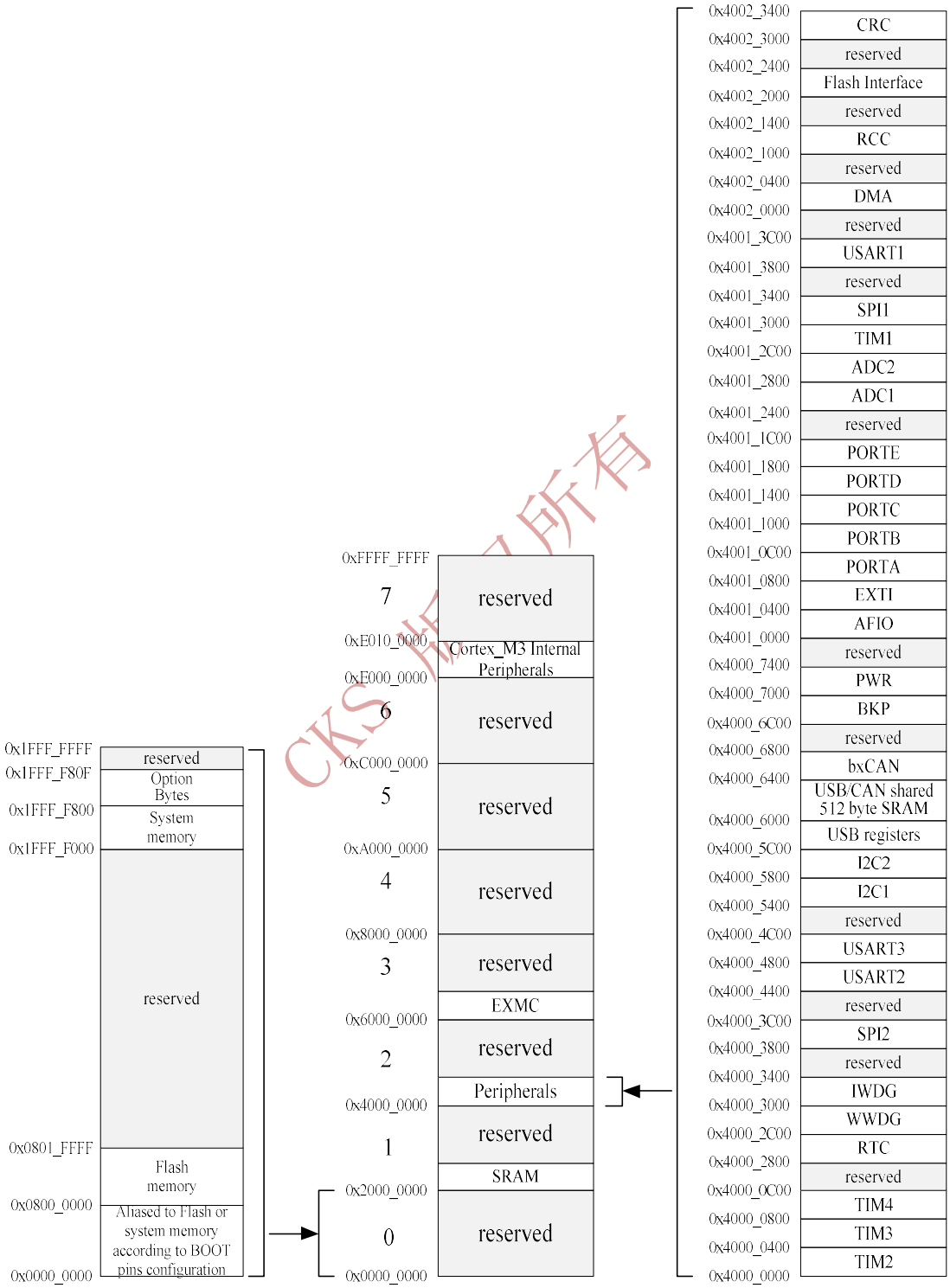


Figure 8 Memory map

# 5. Electrical Characteristics

## 5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 5.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices at an ambient temperature of $T_A$ = 25°C and $T_A$ = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

### 5.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25°C and $V_{DD}$ = 3.3 V (for the 2 V ≤ $V_{DD}$ ≤ 3.3 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

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### 5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in the figure.

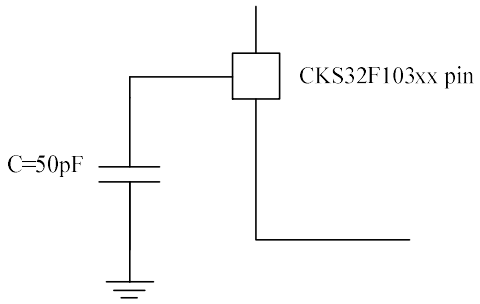


Figure 9 Pin loading conditions

### 5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in the figure.

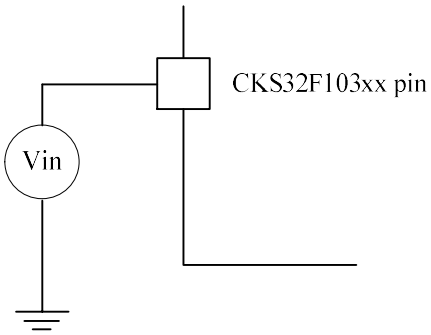


Figure 10 Pin input voltage

### 5.1.6 Power supply schemes

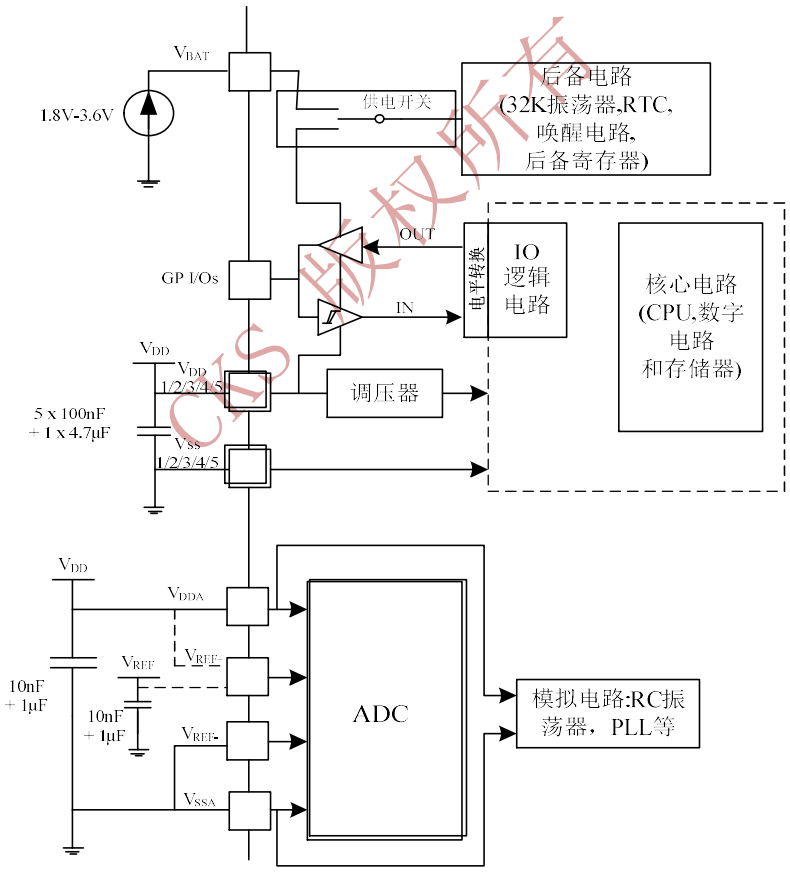


Figure 11 Power supply scheme

Note: The 4.7 µF capacitor in the figure above must be connected to $V_{DD3}$.

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### 5.1.7 Current consumption measurement

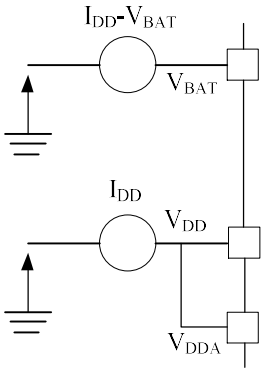


Figure 12 Current consumption measurement scheme

## 5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 3, Table 4 and Table 5 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 3 Voltage characteristics

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD} - V_{SS}$ | External main supply voltage (including $V_{DDA}$ and $V_{DD}$) (1) | -0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on five-volt-tolerant pins(2) | $V_{SS}$ -0.3 | $V_{DD}$ +4.0 | |
| | Input voltage on any other pin(2) | $V_{SS}$ -0.3 | 4.0 | |
| $\|\Delta V_{DDx}\|$ | Variations between different $V_{DD}$ power pins | | 50 | mV |
| $\|V_{SSX} - V_{SS}\|$ | Variations between all the different ground pins | | 50 | |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | See Section 5.3.11 | | |

1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.

2. $I_{INJ(PIN)}$ must never be exceeded (see Table 4), i.e. $V_{IN}$ must not exceed its maximum value. If $V_{IN}$ cannot be kept below its maximum value, the current must be externally limited so that $I_{INJ(PIN)}$ does not exceed its maximum value. A positive injection is induced by $V_{IN} > V_{IN}$max, while a negative injection is induced by $V_{IN} < V_{SS}$.

Table 4 Current characteristics

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}/V_{DDA}$ power lines (source)(1) | 150 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground lines (sink)(1) | 150 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current sourced by any I/O and control pin | -25 | |
| $I_{INJ(PIN)}$(2)(3) | Injected current on five-volt-tolerant pins | -5/+0 | |
| | Injected current on any other pin(4) | ±5 | |
| $\sum I_{INJ(PIN)}$(2) | Total injected current (sum of all I/O and control pins)(4) | ±25 | |

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1. All main power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $I_{INJ(PIN)}$ must never be exceeded, i.e. $V_{IN}$ must not exceed its maximum value. If $V_{IN}$ cannot be kept below its maximum value, the current must be externally limited so that $I_{INJ(PIN)}$ does not exceed its maximum value. A positive injection is induced by $V_{IN} > V_{DD}$, while a negative injection is induced by $V_{IN} < V_{SS}$.
3. Negative injection disturbs the analog performance of the device. See Section 5.3.17.
4. When several inputs are submitted to a current injection, the maximum $I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values). These results are based on characterization with $I_{INJ(PIN)}$ maximum current injection on four I/O port pins of the device.

Table 5 Thermal characteristics

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65~+150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

# 5.3 Operating conditions

## 5.3.1 General operating conditions

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Table 6 General operating conditions

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | | | 0 | 72 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | | | 0 | 36 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | | | 0 | 72 | |
| $V_{DD}$ | Standard operating voltage | | | 2 | 3.6 | V |
| $V_{DDA}$(1) | Analog operating voltage (ADC not used) | Must be the same potential as $V_{DD}$(2) | | 2 | 3.6 | |
| | Analog operating voltage (ADC used) | | | 2.4 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | | | 1.8 | 3.6 | |
| $V_{IN}$ | I/O input voltage | Standard I/O | | -0.3 | $V_{DD}$+0.3 | |
| | | FT I/O | 2V<$V_{DD}$<3.6V | -0.3 | 5.5 | |
| | | | $V_{DD}$=2V | -0.3 | 5.2 | |
| | | BOOT0 | | 0 | 5.5 | |
| $P_D$ | Power dissipation<br>Temperature suffix 6: T = 85°C (suffix 6) or T = 105°C (suffix 7) | LQFP100 | | | 434 | mW |
| | | LQFP64 | | | 444 | |
| | | LQFP48 | | | 363 | |
| | | QFN36 | | | 1000 | |
| $T_A$ | Ambient temperature (suffix 6) | Maximum power dissipation | | -40 | 85 | °C |
| | | Low power dissipation(4) | | -40 | 105 | |
| | Ambient temperature (suffix 7) | Maximum power dissipation | | -40 | 105 | |
| | | Low power dissipation(4) | | -40 | 125 | |

| | | | | | |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature range | Suffix 6 | -40 | 105 | |
| | | Suffix 7 | -40 | 125 | |

1. When the ADC is used, refer to Table 43.

2. It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300 mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and normal operation.
3. If $T_A$ is lower, higher $P_D$ values are allowed as long as $T_J$ does not exceed $T_{J\ max}$ (see Section 1).

4. In low power dissipation state, $T_A$ can be extended to this range as long as $T_J$ does not exceed $T_{Jmax}$ (see Section 1).

### 5.3.2 Operating conditions at power-up/power-down

The parameters given in the table below are derived from tests performed under general operating conditions.

Table 7 Operating conditions at power-up/power-down

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | | 0 | ∞ | μs/V |
| | $V_{DD}$ fall time rate | | 20 | ∞ | |

### 5.3.3 Embedded reset and power control block characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in Table 6.

Table 8 Embedded reset and power control block characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$ | Programmable voltage detector level selection | PLS[2:0] = 000 (rising edge) | 2.10 | 2.18 | 2.26 | V |
| | | PLS[2:0] = 000 (falling edge) | 2.00 | 2.07 | 2.16 | V |
| | | PLS[2:0] = 001 (rising edge) | 2.19 | 2.28 | 2.37 | V |
| | | PLS[2:0] = 001 (falling edge) | 2.09 | 2.17 | 2.27 | V |
| | | PLS[2:0] = 010 (rising edge) | 2.28 | 2.38 | 2.48 | V |
| | | PLS[2:0] = 010 (falling edge) | 2.18 | 2.27 | 2.38 | V |
| | | PLS[2:0] = 011 (rising edge) | 2.38 | 2.47 | 2.58 | V |
| | | PLS[2:0] = 011 (falling edge) | 2.28 | 2.37 | 2.48 | V |
| | | PLS[2:0] = 100 (rising edge) | 2.47 | 2.57 | 2.69 | V |
| | | PLS[2:0] = 100 (falling edge) | 2.37 | 2.46 | 2.59 | V |
| | | PLS[2:0] = 101 (rising edge) | 2.57 | 2.67 | 2.79 | V |
| | | PLS[2:0] = 101 (falling edge) | 2.47 | 2.56 | 2.69 | V |
| | | PLS[2:0] = 110 (rising edge) | 2.66 | 2.77 | 2.90 | V |
| | | PLS[2:0] = 110 (falling edge) | 2.56 | 2.66 | 2.80 | V |
| | | PLS[2:0] = 111 (rising edge) | 2.76 | 2.86 | 3.00 | V |
| | | PLS[2:0] = 111 (falling edge) | 2.66 | 2.76 | 2.90 | V |
| $V_{PVDhyst}$(2) | PVD hysteresis | | | 100 | | mV |
| $V_{POR/PDR}$ | Power-on/power-down | Falling edge | 1.8(1) | 1.87 | 1.96 | V |

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| | | | | | | |
|---|---|---|---|---|---|---|
| | reset threshold | Rising edge | 1.84 | 1.92 | 2.0 | V |
| $V_{PVDhyst}$(2) | PDR hysteresis | | | 40 | | mV |
| $T_{RSTTEMPO}$(2) | Reset temporization | | 1 | 2.5 | 4.5 | ms |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

2. Guaranteed by design, not tested in production.

### 5.3.4 Embedded reference voltage

The parameters given in the table below are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in Table 6.

Table 9 Embedded internal reference voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | -40°C < $T_A$< +85°C | 1.16 | 1.20 | 1.24 | V |
| $T_{S_vrefint}$(1) | ADC sampling time when reading the internal reference voltage | | | 5.1 | 17.1(2) | μs |

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.

2. Guaranteed by design, not tested in production.

### 5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors, such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in the figure.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

#### Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above 48 MHz).
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling).
- When the peripherals are enabled: $f_{PCLK1} = f_{HCLK/2}$, $f_{PCLK2} = f_{HCLK}$.

The parameters given in Table 10, Table 11 and Table 12 are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in Table 5.

Table 10 Maximum current consumption in Run mode, code with data processing running from Flash

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode, $T_A$ = 85°C | External clock(2), all peripherals enabled | 72MHz | 50 | mA |
| | | | 48MHz | 36.1 | |
| | | | 36MHz | 28.6 | |

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| | | | | | |
|---|---|---|---|---|---|
| | | | 24MHz | 19.9 | |
| | | | 16MHz | 14.7 | |
| | | | 8MHz | 8.6 | |
| | | External clock(2), all peripherals disabled | 72MHz | 32.8 | |
| | | | 48MHz | 24.4 | |
| | | | 36MHz | 19.8 | |
| | | | 24MHz | 13.9 | |
| | | | 16MHz | 10.7 | |
| | | | 8MHz | 6.8 | |

1. Based on characterization, not tested in production.

2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 11 Maximum current consumption in Run mode, code with data processing running from RAM

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Supply current in Run mode, $T_A$ = 85°C | External clock(2), all peripherals enabled | 72MHz | 48 | mA |
| | | | 48MHz | 31.5 | |
| | | | 36MHz | 24 | |
| | | | 24MHz | 17.5 | |
| | | | 16MHz | 12.5 | |
| | | | 8MHz | 7.5 | |
| | | External clock(2), all peripherals disabled | 72MHz | 29 | |
| | | | 48MHz | 20.5 | |
| | | | 36MHz | 16 | |
| | | | 24MHz | 11.5 | |
| | | | 16MHz | 8.5 | |
| | | | 8MHz | 5.5 | |

1. Based on characterization, tested in production at $V_{DD}$max and $f_{HCLK}$max.

2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 12 Maximum current consumption in Sleep mode, code running from Flash or RAM

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | Unit |
|---|---|---|---|---|---|
| | | | | $T_A$= 85°C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(2), all peripherals enabled | 72MHz | 30 | mA |
| | | | 48MHz | 20 | |
| | | | 36MHz | 15.5 | |
| | | | 24MHz | 11.5 | |
| | | | 16MHz | 8.5 | |

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| | | | | | |
|---|---|---|---|---|---|
| | | | 8MHz | 22 | |
| | | External clock(2), all peripherals disabled | 72MHz | 7.5 | |
| | | | 48MHz | 6 | |
| | | | 36MHz | 5 | |
| | | | 24MHz | 4.5 | |
| | | | 16MHz | 4 | |
| | | | 8MHz | 3 | |

1. Based on characterization, tested in production at $V_{DD}$max and $f_{HCLK}$max with peripherals enabled.

2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 13 Typical and maximum current consumption in Stop and Standby modes

| Symbol | Parameter | Conditions | Typ | | | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | | $V_{DD}/V_{BAT}$= 2.4V | $V_{DD}/V_{BAT}$= 3.3V | $V_{DD}/V_{BAT}$ = 3.6V | $T_A$= 85°C | |
| $I_{DD}$ | Supply current in Stop mode | Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 22.7 | 23.4 | 20 | 200 | μA |
| | | Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog) | 9.1 | 10.3 | - | 180 | |
| | Supply current in Standby mode | Low-speed internal RC oscillator and independent watchdog ON | 2.65 | 3.58 | 3.85 | - | |
| | | Low-speed internal RC oscillator ON, independent watchdog OFF | 2.62 | 3.39 | 3.72 | - | |
| | | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | 1.64 | 2.09 | 2.29 | 4 | |
| $I_{DD_VBAT}$ | Backup domain supply current | Low-speed oscillator and RTC ON state | 1.1 | 1.4 | - | 1.9(2) | |

1. Typical values are measured at $T_A$ = 25°C.

2. Based on characterization, not tested in production.

## Typical current consumption

The MCU is placed under the following conditions:

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- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above 48 MHz).
- Ambient temperature and $V_{DD}$ supply voltage conditions are summarized in Table 6.
- Prefetch is on (reminder: this bit must be set before clock setting and bus prescaling). When the peripherals are enabled: $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK2} = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$.

Table 14 Typical current consumption in Run mode, code with data processing running from internal Flash

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled(2) | All peripherals disabled | |
| $I_{DD}$ | Supply current in Run mode | External clock(3) | 72MHz | 32.46 | 21.7 | mA |
| | | | 48MHz | 21.96 | 14.73 | |
| | | | 24MHz | 12.13 | 8.57 | |
| | | | 8MHz | 5.5 | 4.31 | |

1. Typical values are measured at $T_A = 25°C$, $V_{DD} = 3.3$ V.

2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

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Table 15 Typical current consumption in Run mode, code with data processing running from internal RAM

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled(2) | All peripherals disabled | |
| $I_{DD}$ | Supply current in Run mode | External clock(3) | 72MHz | 24.84 | 14.21 | mA |
| | | | 48MHz | 17.17 | 10.05 | |
| | | | 24MHz | 9.38 | 5.86 | |
| | | | 8MHz | 4.07 | 2.92 | |

1. Typical values are measured at $T_A = 25°C$, $V_{DD} = 3.3$ V.

2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 16 Typical current consumption in Sleep mode, code running from internal Flash or RAM

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled(2) | All peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(3) | 72MHz | 18.18 | 17.57 | mA |

1. Typical values are measured at $T_A = 25°C$, $V_{DD} = 3.3$ V.

2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).

3. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in Table 17. The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are disabled except when explicitly mentioned.
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient temperature and $V_{DD}$ supply voltage conditions are summarized in Table 4.

Table 17 Peripheral current consumption(1)

| Peripheral | | Typical consumption at 25°C | Unit | Peripheral | | Typical consumption at 25°C | Unit |
|---|---|---|---|---|---|---|---|
| APB1 | TIM2 | 1.2 | mA | APB2 | GPIOA | 0.47 | mA |
| | TIM3 | 1.2 | | | GPIOB | 0.47 | |
| | TIM4 | 0.9 | | | GPIOC | 0.47 | |
| | SPI2 | 0.2 | | | GPIOD | 0.47 | |
| | USART2 | 0.35 | | | GPIOE | 0.47 | |
| | USART3 | 0.35 | | | ADC1(2) | 1.81 | |
| | $I^2C1$ | 0.39 | | | ADC2 | 1.78 | |
| | $I^2C2$ | 0.39 | | | TIM1 | 1.6 | |
| | USB | 0.65 | | | SPI1 | 0.43 | |
| | CAN | 0.72 | | | USART1 | 0.85 | |

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1. $f_{HCLK}$ = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.

2. Specific conditions for ADC: $f_{HCLK}$ = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$, ADON bit in the ADC_CR2 register set to 1.

## 5.3.6 External clock source characteristics

### High-speed external user clock generated from an external source

The characteristics given in the table below result from tests performed using a high-speed external clock source, under the ambient temperature and supply voltage conditions summarized in Table 6.

Table 18 High-speed external user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE_ext}$ | User external clock source frequency(1) | | 7.95 | 8 | 8.05 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high-level voltage | | 2.2 | | 3.3 | V |
| $V_{HSEL}$ | OSC_IN input pin low-level voltage | | 0 | | 2.2 | |
| $t_{w(HSE)}$ | OSC_IN high or low time(1) | | 5 | | | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{w(HSE)}$ | | | | | | |
| $t_{r(HSE)}$<br>$t_{f(HSE)}$ | OSC_IN rise or fall time(1) | | | | 20 | |
| $C_{in(HSE)}$ | OSC_IN input capacitance(1) | | | 5 | | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | 45 | 50 | 55 | % |
| $I_L$ | OSC_IN input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | | 0.3 | ±1 | μA |

1. Guaranteed by design, not tested in production.

## Low-speed external user clock generated from an external source

The characteristics given in the table below result from tests performed using a low-speed external clock source, under the ambient temperature and supply voltage conditions summarized in Table 6.

Table 19 Low-speed external user clock characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE_ext}$ | User external clock source frequency(1) | | 31 | 32.768 | 33 | KHz |
| $V_{LSEH}$ | OSC32_IN input pin high-level voltage | | 1.8 | | 3.3 | V |
| $V_{LSEL}$ | OSC32_IN input pin low-level voltage | | 0 | | 1.7 | |
| $t_{w(LSE)}$<br>$t_{w(LSE)}$ | OSC32_IN high or low time(1) | | 450 | | | ns |
| $t_{r(LSE)}$<br>$t_{f(LSE)}$ | OSC32_IN rise or fall time(1) | | | | 50 | |
| $C_{in(LSE)}$ | OSC32_IN input capacitance(1) | | | 5 | | pF |
| $DuCy_{(LSE)}$ | Duty cycle | | 30 | 50 | 70 | % |
| $I_L$ | OSC32_IN input leakage current | $V_{SS} \le V_{IN} \le V_{DD}$ | | -0.4 | ±1 | μA |

1. Guaranteed by design, not tested in production.

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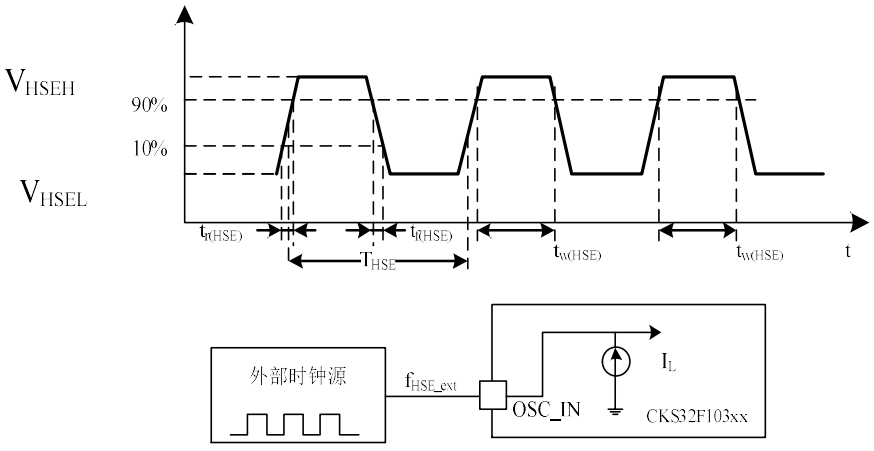


Figure 13 High-speed external clock source AC timing diagram

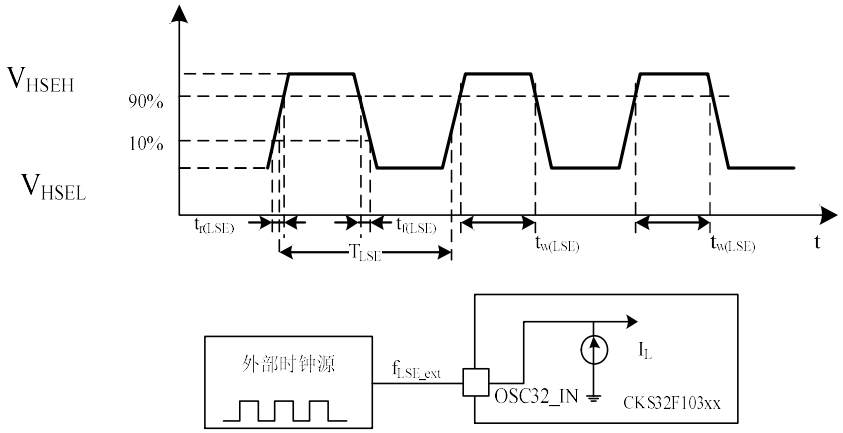


Figure 14 Low-speed external clock source AC timing diagram

## High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this section is based on characterization results obtained with the typical external components specified in the table below. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Table 20 HSE 4-16 MHz oscillator characteristics(1)(2)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC_IN}$ | Oscillator frequency | | 4 | 8 | 16 | MHz |
| $R_F$ | Feedback resistor | | | 200 | | kΩ |
| $C_{L1}$<br>$C_{L2}$(3) | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(4) | $R_s$= 30Ω | | 30 | | pF |
| $i_2$ | HSE driving current | $V_{DD}$ = 3.3 V, $V_{IN}$ = $V_{SS}$ with 30 pF load | | | 1 | mA |
| $g_m$ | Oscillator transconductance | Startup | 25 | | | mA/V |
| $t_{SU(HSE)}$(5) | Startup time | $V_{DD}$ is stabilized | | 2 | | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

2. Based on characterization, not tested in production.

3. For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. PCB and MCU pin capacitance must be included when sizing $C_{L1}$ and $C_{L2}$ (10 pF can be used as a rough estimate of the combined pin and board capacitance).

4. The relatively low value of the RF resistor offers good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.

5. $t_{SU(HSE)}$ is the startup time measured from the moment HSE is enabled by software until a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

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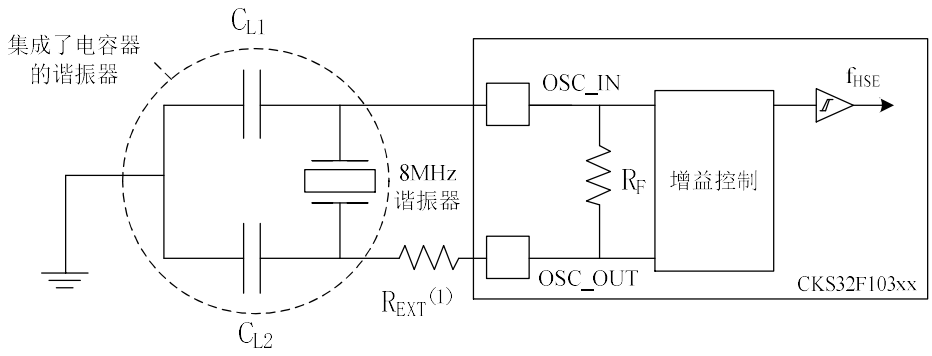


Figure 15 Typical application with an 8 MHz crystal

1. The value of $R_{EXT}$ depends on the crystal characteristics. Typical value is 5 to 6 times $R_S$.

## Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this section is based on characterization results obtained with the typical external components specified in Table 21. In the application, the resonator and the load capacitors must be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time.

Note: For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range, selected to match the requirements of the crystal or resonator.

$C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$.

Load capacitance $C_L$ has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where $C_{stray}$ is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of $C_{L1}$ and $C_{L2}$ (15 pF), it is strongly recommended to use a resonator with a load capacitance $C_L \leq 7$ pF. Never use a resonator with a load

capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of $C_L = 6$ pF and $C_{stray} = 2$ pF, then $C_{L1} = C_{L2} = 8$ pF.

Table 21 LSE oscillator characteristics ($f_{LSE}$ = 32.768 kHz)(1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_F$ | Feedback resistor | | | 5 | | MΩ |
| $C_{L1}$<br>$C_{L2}$(2) | Recommended load capacitance versus equivalent serial resistance of the crystal ($R_S$)(3) | $R_S$= 30kΩ | | | 15 | pF |
| $I_2$ | LSE driving current | $V_{DD}$=3.3V, $V_{IN}$=$V_{SS}$ | | | 1.4 | μA |
| $g_m$ | Oscillator transconductance | | 5 | | | μA/V |
| $t_{SU(LSE)}$(4) | Startup time | $V_{DD}$ is stabilized | | 3 | | s |

1. Based on characterization, not tested in production.

2. See the note and caution paragraphs above this table.

3. Current consumption can be optimized by choosing a high-quality resonator with a small $R_S$ value (e.g. MSIV-TIN32.768kHz).

4. $t_{SU(HSE)}$ is the startup time measured from the moment HSE is enabled by software until a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

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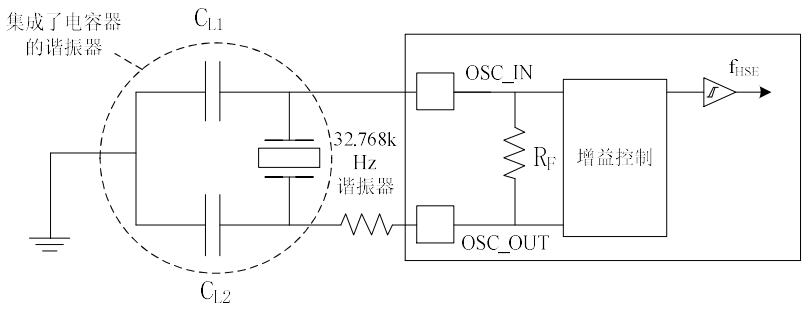


Figure 16 Typical application with a 32.768 kHz crystal

## 5.3.7 Internal clock source characteristics

The parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 6.

### High-speed internal (HSI) RC oscillator

Table 22 HSI oscillator characteristics(1)(2)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | | 7.95 | 8.0 | 8.05 | MHz |
| $ACC_{HSI}$ | Accuracy of the HSI oscillator | $T_A$= -10~85°C | -1.5 | | 2.2 | % |
| | | $T_A$= 0~70°C | -1.3 | | 2 | % |
| | | $T_A$= 25°C | -1.1 | | 1.8 | % |
| $t_{SU(HSI)}$ | HSI oscillator startup time | | 1 | | 2 | μs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 80 | 100 | μA |

1. $V_{DD}$ = 3.3 V, $T_A$ = -40 to 85°C unless otherwise specified.

2. Guaranteed by design, not tested in production.

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### Low-speed internal (LSI) RC oscillator

Table 23 LSI oscillator characteristics(1)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{LSI}$(2) | Frequency | 39 | 44.74 | 49 | kHz |
| $t_{SU(LSI)}$(3) | LSI oscillator startup time | | | 85 | μs |
| $I_{DD(LSI)}$(3) | LSI oscillator power consumption | | 0.65 | 1.2 | μA |

1. $V_{DD}$ = 3.3 V, $T_A$ = -40 to 85°C unless otherwise specified.

2. Based on characterization, not tested in production.

3. Guaranteed by design, not tested in production.

### Wakeup time from low-power mode

The wakeup times given in Table 24 are measured on a wakeup phase with an 8 MHz HSI RC oscillator. The clock source used to wake up the device depends on the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator

- Sleep mode: the clock source is the clock that was set before entering Sleep mode

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 6.

Table 24 Low-power mode wakeup timings

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $t_{WUSLEEP}$(1) | Wakeup from Sleep mode | Wakeup on HSI RC clock | 1.7 | µs |
| $t_{WUSTOP}$(1) | Wakeup from Stop mode (regulator in run mode) | HSI RC wakeup time = 2 µs | 2.6 | |
| | Wakeup from Stop mode (regulator in low-power mode) | HSI RC wakeup time = 2 µs<br>Regulator wakeup from low-power mode time = 5 µs | 5.1 | |
| $t_{WUSTDBY}$(3) | Wakeup from Standby mode | HSI RC wakeup time = 2 µs<br>Regulator wakeup from power-down time = 38 µs | 52 | |

1. The wakeup times are measured from the wakeup event to the point at which the user application code reads the first instruction.

## 5.3.8 PLL characteristics

The parameters given in Table 25 are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 6.

Table 25 PLL characteristics

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $f_{PLL_IN}$ | PLL input clock(2) | 9.9 | - | 10.1 | MHz |
| | PLL input clock duty cycle | 40 | 50 | 60 | % |
| $f_{PLL_OUT}$ | PLL multiplier output clock | 16 | | 72 | MHz |
| $t_{LOCK}$ | PLL lock time | | 43 | 200 | µs |

1. Based on characterization, not tested in production.

2. Take care to use the appropriate multiplier factor so as to obtain a PLL output frequency $f_{PLL_OUT}$ within the allowed range, depending on the PLL input clock frequency.

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## 5.3.9 Memory characteristics

### Flash memory

The characteristics are given at $T_A$ = -40 to 85°C unless otherwise specified.

Table 26 Flash memory characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | 16-bit programming time | $T_A$= -40~85°C | - | - | 20 | µs |
| $t_{ERASE}$ | Page (1 KB) erase time | $T_A$= -40~85°C | - | | 2 | ms |
| $t_{ME}$ | Mass erase time | $T_A$= -40~85°C | - | | 10 | |
| $I_{DD}$ | Supply current | Read mode, $f_{HCLK}$ = 72 MHz with 2 wait states, VDD=3.3V | | | 21.6 | mA |
| | | Write/erase mode, $f_{HCLK}$ = 72 MHz, VDD = 3.3 V | | | 3 | |
| | | Standby mode, VDD = 3.3 to 3.6 V | | | 1 | µA |

1. Guaranteed by design, not tested in production.

Table 27 Flash memory endurance and data retention

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = -40 to 85°C (suffix 6) | 10 | | | kcycles |
| $t_{RET}$ | Data retention | at $T_A$ = -40 to 85°C | 10 | | | Years |

1. Based on characterization, not tested in production.

## 5.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs.

- **Electrostatic discharge (ESD) (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.**
- **FTB: a burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.**

A device reset allows normal operation to be resumed.

The test results are given in the table below.

Table 28 EMS characteristics

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz. Conforms to IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{HCLK}$ = 72 MHz. Conforms to IEC 61000-4-4 | 4A |

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for the application.

### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical data corruption (control registers, etc.)

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### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors from occurring.

### Electromagnetic interference (EMI)

The electromagnetic field emitted by the device is monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with the SAE J1752/3 standard, which specifies the test board and the pin loading.

Table 29 EMI characteristics

| Symbol | Parameter | Conditions | Monitored frequency band | Max ($f_{HSE}/f_{HCLK}$) | | Unit |
|---|---|---|---|---|---|---|
| | | | | 8/48MHz | 8/72MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.3 V, $T_A$ = 25°C, LQFP100 package, compliant with IEC 61967-2 | 0.1~30MHz | 12 | 12 | dBμV |
| | | | 30~130MHz | 22 | 19 | |
| | | | 130MHz~1GHz | 23 | 29 | |
| | | | SAE EMI level | 4 | 4 | - |

## 5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 30 ESD absolute maximum ratings

| Symbol | Parameter | Conditions | Type | Max(1) | Unit |
|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | T = +25 °C, conforming to JESD22-A114 | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | T = +25 °C, conforming to JESD22-C101 | II | 500 | |

1. Based on characterization, not tested in production.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

This test conforms to the EIA/JESD 78A IC latch-up standard.

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Table 31 Electrical sensitivities

| Symbol | Parameter | Conditions | Type |
|---|---|---|---|
| LU | Static latch-up class | T = +85 °C, conforming to JESD78A | II class A |

## 5.3.12 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the conditions summarized in Table 6. All I/Os are CMOS- and TTL-compliant.

Table 32 I/O static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage | Standard I/O input low-level voltage | - | - | $0.28\times(V_{DD}-2V)+0.8V$ | V |
| | | FT I/O(1) input low-level voltage | | | $0.32\times(V_{DD}-2V)+0.75V$ | |
| | | All I/Os except BOOT0 | | | $0.35\ V_{DD}$ | |
| $V_{IH}$ | High-level input voltage | Standard I/O input high-level voltage | $0.41\times(V_{DD}-2V)+1.3V$ | | | |
| | | FT I/O(1) input high-level voltage | $0.42\times(V_{DD}-2V)+1V$ | | | |
| | | All I/Os except BOOT0 | $0.65\ V_{DD}$(2) | | | |
| $V_{hys}$ | Standard I/O Schmitt trigger voltage hysteresis(2) | | 200 | | | mV |
| | 5 V-tolerant I/O Schmitt trigger voltage hysteresis (2) | | $5\%V_{DD}$(3) | | | |
| $I_{lkg}$ | Input leakage current(4) | $V_{SS} \le V_{IN} \le V_{DD}$, standard I/Os | | | ±1 | µA |
| | | $V_{IN}$ = 5 V, 5 V-tolerant I/Os | | | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor(5) | $V_{IN} = V_{SS}$ | 30 | 44 | 50 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(5) | $V_{IN} = V_{DD}$ | 30 | 44 | 50 | |
| $C_{IO}$ | I/O pin capacitance | | | 5 | | pF |

1. FT = Five-volt tolerant.
2. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than the maximum if negative current is injected on adjacent pins.

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5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/ NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL
parameters:

- For $V_{IH}$:
  - If $V_{DD}$ is in [2.00 V - 3.08 V]: CMOS characteristics, but TTL included.
  - If $V_{DD}$ is in [3.08 V - 3.60 V]: TTL characteristics, but CMOS included.
- For $V_{IL}$:
  - If $V_{DD}$ is in [2.00 V - 2.28 V]: TTL characteristics, but CMOS included.
  - If $V_{DD}$ is in [2.28 V - 3.60 V]: CMOS characteristics, but TTL included.

## Output driving current

The GPIOs (general-purpose inputs/outputs) can sink or source up to ±8 mA, and sink +20 mA (with a relaxed $V_{OL}$).

In the user application, the number of I/O pins must be limited so that the driving current respects the absolute maximum ratings given in Section 5.2:

- The sum of the currents sourced by all the I/Os on $V_{DD}$, plus the maximum Run consumption of the MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating IVDD (see Table 4).
- The sum of the currents sunk by all the I/Os on $V_{SS}$, plus the maximum Run consumption of the MCU sunk on $V_{SS}$, cannot exceed the absolute maximum rating IVSS (see Table 4).

## Output voltage levels

Unless otherwise specified, the parameters given in Table 33 are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in Table 6. All I/Os are CMOS- and TTL-compliant.

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Table 33 Output voltage characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}^{(1)}$ | Output low-level voltage, 8 pins sunk simultaneously | CMOS port, $I_{IO}$ = +8 mA | | 0.4 | V |
| $V_{OH}^{(2)}$ | Output high-level voltage, 8 pins sourced simultaneously | 2.7V < $V_{DD}$< 3.6V | $V_{DD}$-0.4 | | |
| $V_{OL}^{(1)}$ | Output low-level voltage, 8 pins sunk simultaneously | TTL port, $I_{IO}$ = +8 mA | | 0.4 | |
| $V_{OH}^{(2)(3)}$ | Output high-level voltage, 8 pins sourced simultaneously | 2.7V < $V_{DD}$< 3.6V | 2.4 | | |
| $V_{OL}^{(1)(3)}$ | Output low-level voltage, 8 pins sunk simultaneously | $I_{IO}$ = +20mA | | 1.3 | |
| $V_{OH}^{(2)(3)}$ | Output high-level voltage, 8 pins sourced simultaneously | 2.7V < $V_{DD}$< 3.6V | 2.4 | | |
| $V_{OL}^{(1)(3)}$ | Output low-level voltage, 8 pins sunk simultaneously | $I_{IO}$ = +6mA | | 0.4 | |
| $V_{OH}^{(2)(3)}$ | Output high-level voltage, 8 pins sourced simultaneously | 2V < $V_{DD}$< 2.7V | $V_{DD}$-0.4 | | |

1. The $I_{IO}$ current sunk by the device must always respect the absolute maximum rating specified in Table 4, and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. The $I_{IO}$ current sourced by the device must always respect the absolute maximum rating specified in Table 4, and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.
3. Based on characterization, not tested in production.

## Input/output AC characteristics

The definition and values of input/output AC characteristics are given in the figure and in Table 34, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in Table 6.

Table 34 I/O AC characteristics (1)

| MODEx[1:0] | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 10 (2MHz) | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$= 50 pF,$V_{DD}$= 2~3.6V | | 2 | MHz |
| | $t_{f(IO)out}$ | Output high-to-low level fall time | $C_L$= 50 pF,$V_{DD}$= 2~3.6V | | 125(3) | ns |
| | $t_{r(IO)out}$ | Output low-to-high level rise time | | | 125(3) | |
| 01 (10MHz) | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$= 50 pF,$V_{DD}$= 2~3.6V | | 10 | MHz |
| | $t_{f(IO)out}$ | Output high-to-low level fall time | $C_L$= 50 pF,$V_{DD}$= 2~3.6V | | 25(3) | ns |
| | $t_{r(IO)out}$ | Output low-to-high level rise time | | | 25(3) | |
| 11 (50MHz) | $f_{max(IO)out}$ | Maximum frequency(2) | $C_L$= 30 pF,$V_{DD}$= 2.7~3.6V | | 50 | MHz |
| | | | $C_L$= 50 pF,$V_{DD}$= 2.7~3.6V | | 30 | |
| | | | $C_L$=50 pF,$V_{DD}$= 2~2.7V | | 20 | |
| | $t_{f(IO)out}$ | Output high-to-low level fall time | $C_L$= 30 pF,$V_{DD}$= 2.7~3.6V | | 5(3) | ns |
| | | | $C_L$= 50 pF,$V_{DD}$= 2.7~3.6V | | 8(3) | |
| | | | $C_L$=50 pF,$V_{DD}$= 2~2.7V | | 12(3) | |
| | $t_{r(IO)out}$ | Output low-to-high level rise time | $C_L$= 30 pF,$V_{DD}$= 2.7~3.6V | | 5(3) | |
| | | | $C_L$= 50 pF,$V_{DD}$= 2.7~3.6V | | 8(3) | |
| | | | $C_L$=50 pF,$V_{DD}$= 2~2.7V | | 12(3) | |
| - | $t_{EXTIpw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | | ns |

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the description of the GPIO port configuration register in the CKS32F103x8 and CKS32F103xB reference manual.

2. The maximum frequency is defined in the figure.

3. Guaranteed by design, not tested in production.

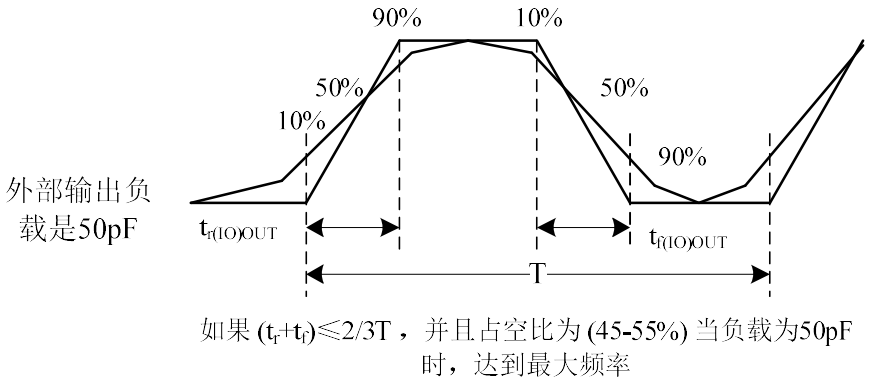


Figure 17 I/O AC characteristics definition

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### 5.3.13 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see Table 32).

Unless otherwise specified, the parameters given in Table 35 are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in Table 6.

Table 35 NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST input low-level voltage | | -0.5 | | 0.8 | V |
| $V_{IH(NRST)}$(1) | NRST input high-level voltage | | 2 | | $V_{DD}$+0.5 | |
| $V_{hys(NRST)}$(1) | NRST Schmitt trigger voltage hysteresis | | | 200 | | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(2) | $V_{IN}$=$V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(1) | NRST input filtered pulse | | | | 100 | ns |
| $V_{NF(NRST)}$(1) | NRST input not-filtered pulse | | 300 | | | ns |

1. Guaranteed by design, not tested in production.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

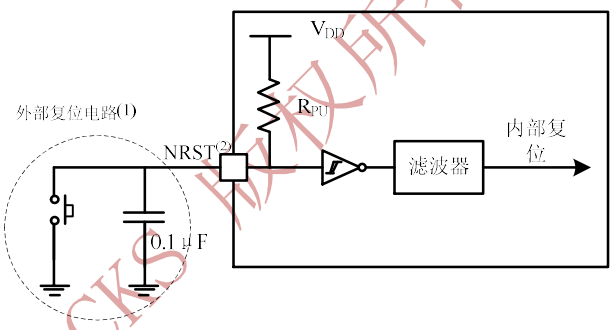


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Figure 18 Recommended NRST pin protection

1. The reset network protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the maximum $V_{IL(NRST)}$ level specified in Table 35; otherwise the reset will not be taken into account by the device.

### 5.3.14 TIM timer characteristics

The parameters given in Table 36 are guaranteed by design.

Refer to Section 5.3.12 for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 36 TIMx(1) characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$= 72MHz | 13.9 | | ns |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}$/2 | MHz |
| | | $f_{TIMxCLK}$ = 72MHz | 0 | 36 | MHz |
| $Res_{TIM}$ | Timer resolution | | | 16 | bit |

| | | | | | |
|---|---|---|---|---|---|
| $t_{COUNTER}$ | 16-bit counter clock period when the internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$= 72MHz | 0.0139 | 910 | μs |
| $t_{MAX_COUNT}$ | Maximum possible count | | | 65536x65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$= 72MHz | | 59.6 | s |

1. TIMx is a generic name standing for TIM1 to TIM4.

## 5.3.15 Communication interfaces

### I²C interface characteristics

Unless otherwise specified, the parameters given in Table 37 are derived from tests performed under the ambient temperature, $f_{PCLK1}$ frequency and $V_{DD}$ supply voltage conditions summarized in Table 6.

The I²C interface of the CKS32F103x8 and CKS32F103xB mainstream devices meets the requirements of the standard I²C communication protocol with the following restriction: SDA and SCL are not "true" open-drain pins. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

The I²C characteristics are given in Table 37. Refer to Section 5.3.12 for details on the input/output alternate function characteristics (SDA and SCL).

Table 37 I²C characteristics

| Symbol | Parameter | Standard-mode I²C(1) | | Fast-mode I²C(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Max | Min | Max | Min | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | μs |
| $t_{wSCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0(3) | | 0(4) | 900(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | 20+0.1$C_b$ | 300 | |
| $t_{fSDA)}$ $t_{fSCL)}$ | SDA and SCL fall time | | 300 | | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | μs |
| $t_{su(STA)}$ | Repeated start condition setup time | 4.7 | | 0.6 | | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | μs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | | 1.3 | | μs |
| $C_b$ | Capacitive load for each bus line | | 400 | | 400 | pF |

1. Guaranteed by design, not tested in production.

2. $f_{PCLK1}$ must be higher than 2 MHz to achieve the maximum standard-mode I²C frequency, and higher than 4 MHz to achieve the maximum fast-mode I²C frequency.

3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of the SCL signal.

4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

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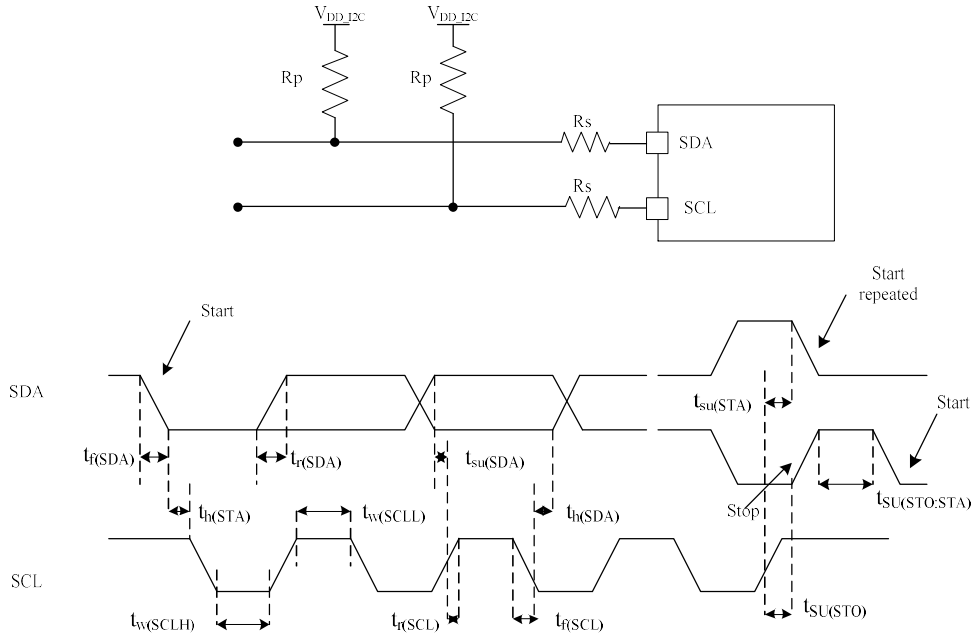


Figure 19 I²C bus AC waveforms and measurement circuit(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 38 SCL frequency ($f_{PCLK1}$ = 36 MHz, $V_{DD}$ = 3.3 V)(1)(2)

| $f_{SCL(kHz)}$ | I²C_CCR value |
|---|---|
| | $R_P$=4.7 kΩ |
| 400 | 0x801E |
| 300 | 0x8028 |
| 200 | 0x803C |
| 100 | 0x00B4 |
| 50 | 0x0168 |
| 20 | 0x0384 |

1. $R_P$ = external pull-up resistance, $f_{SCL}$ = I²C speed.

2. For speeds around 200 kHz, the tolerance on the achieved speed is ±5%. For other speed ranges, the tolerance is ±2%. These variations depend on the accuracy of the external components used in the design.

## SPI interface characteristics

Unless otherwise specified, the parameters given in Table 39 are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in Table 6.

Refer to Section 5.3.12 for details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 39 SPI characteristics(1)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 18 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 8 | ns |

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| | | | | | |
|---|---|---|---|---|---|
| Ducy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$(2) | NSS setup time | Slave mode | $4t_{PCLCK}$ | - | ns |
| $t_{h(NSS)}$(2) | NSS hold time | Slave mode | $2t_{PCLCK}$ | - | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, prescaler = 4 | 50 | 60 | |
| $t_{su(MI)}$(2)<br>$t_{su(SI)}$(2) | Data input setup time, master mode | Master mode | 5 | | |
| | | Slave mode | 5 | | |
| $t_{h(MI)}$(2)<br>$t_{h(SI)}$(2) | Data input hold time, master mode | Master mode | 5 | | |
| | | Slave mode | 4 | | |
| $t_{a(SO)}$(2)(3) | Data output access time | Slave mode, $f_{PCLK}$ = 20 MHz | 0 | $3t_{PCLCK}$ | |
| $t_{dis(SO)}$(2)(4) | Data output disable time | Slave mode | 2 | 10 | |
| $t_{v(SO)}$(2)(1) | Data output valid time | Slave mode (after enable edge) | | 25 | |
| $t_{v(MO)}$(2)(1) | Data output valid time | Master mode (after enable edge) | | 5 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode (after enable edge) | 15 | | |
| $t_{h(MO)}$(2) | | Master mode (after enable edge) | 2 | | |

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output; max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output; max time is for the maximum time to put the data in Hi-Z.

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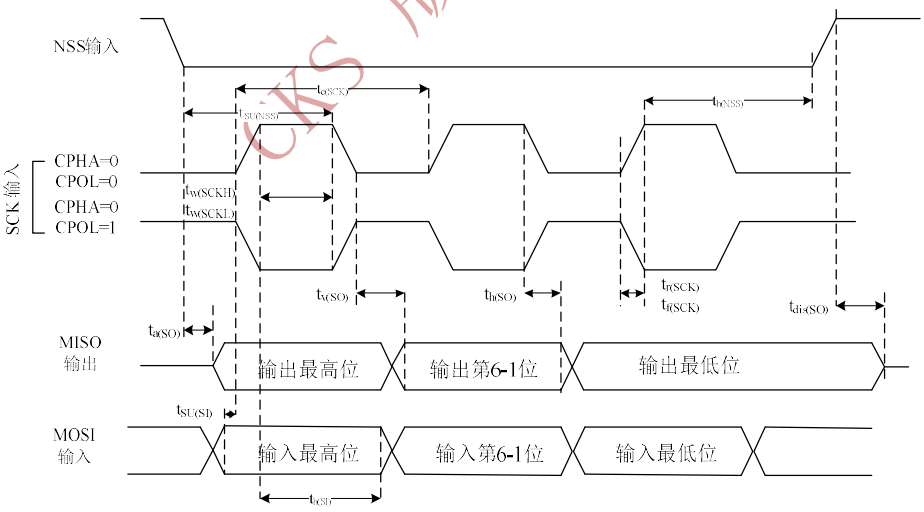


Figure 20 SPI timing diagram - slave mode and CPHA = 0

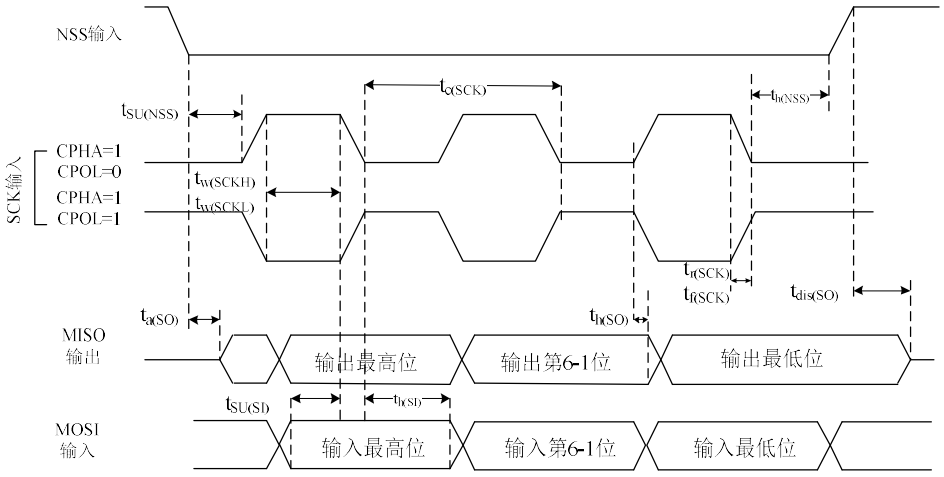


Figure 21 SPI timing diagram - slave mode and CPHA = 1(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

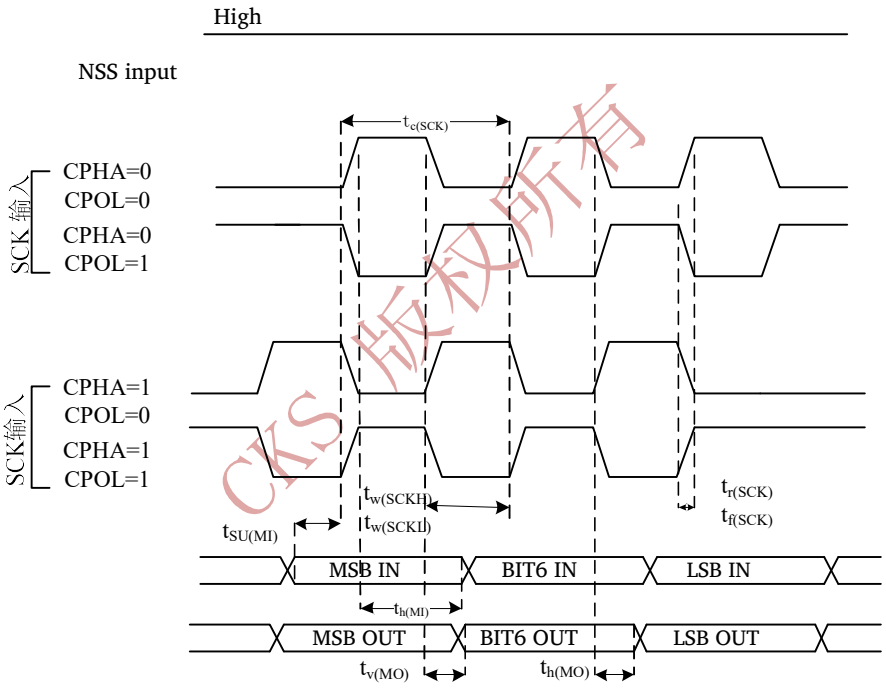


Figure 22 SPI timing diagram - master mode(1)

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

## USB characteristics

The USB (full-speed) interface is USB-IF certified.

Table 40 USB startup time

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB transceiver startup time | 1 | μs |

1. Guaranteed by design, not tested in production.

Table 41 USB DC electrical characteristics

| Symbol | Parameter | Conditions | Min(1) | Max(1) | Unit |
|---|---|---|---|---|---|
| Input levels | | | | | |

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| | | | | | |
|---|---|---|---|---|---|
| $V_{DD}$ | USB operating voltage(2) | | 3.0(3) | 3.6 | V |
| $V_{DI}$(4) | Differential input sensitivity | I(USBDP,USBDM) | 0.2 | | V |
| $V_{CM}$(4) | Differential common-mode range | Includes $V_{DI}$ range | 0.8 | 2.5 | |
| $V_{SE}$(4) | Single-ended receiver threshold | | 1.3 | 2.0 | |
| Output levels | | | | | |
| $V_{OL}$ | Static output level low | $R_L$ of 1.5 kΩ to 3.6 V(5) | | 0.3 | V |
| $V_{OH}$ | Static output level high | $R_L$ of 15 kΩ to $V_{SS}$(5) | 2.8 | 3.6 | |

1. All voltages are measured from the local ground potential.

2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP (D+) pin should be pulled up with a 1.5 kΩ resistor to a 3.0-to-3.6 V voltage range.
3. The CKS32F0103xx correct USB functionality is ensured down to 2.7 V, but not the full USB electrical characteristics, which are degraded in the 2.7-to-3.0 V voltage range.
4. Guaranteed by characterization, not tested in production.

5. $R_L$ is the load connected on the USB drivers.

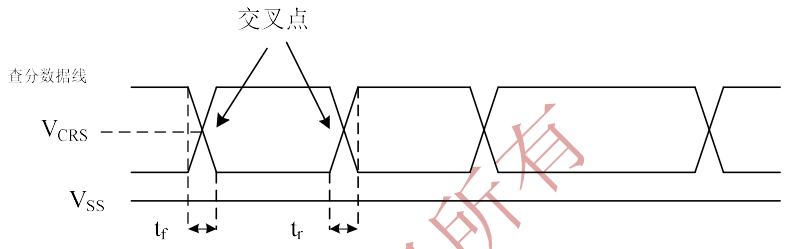


Figure 23 USB timings: definition of data signal rise and fall time

Table 42 USB full-speed electrical characteristics(1)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_r$ | Rise time(2) | CL ≤ 50pF | 4 | 20 | ns |
| $t_f$ | Fall time(2) | CL ≤ 50pF | 4 | 20 | ns |
| $t_{rfm}$ | Rise/fall time matching | $t_r$ / $t_f$ | 90 | 110 | % |
| $V_{CRS}$ | Output signal crossover voltage | | 1.3 | 2.0 | V |

1. Guaranteed by design, not tested in production.

2. Measured from 10% to 90% of the data signal.

## 5.3.16 CAN (controller area network) interface

Refer to Section 5.3.12 for details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

## 5.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters in Table 43 are measured using ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in Table 6.

Note: It is recommended to perform a calibration after each power-up.

Table 43 ADC characteristics

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| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | - | 2.4 | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | - | 2.4 | - | $V_{DDA}$ | V |
| $I_{VREF}$ | Voltage on the $V_{REF+}$ input pin | - | - | 160(1) | 220(1) | μA |
| $f_{ADC}$ | ADC clock frequency | - | 0.6 | - | 14 | MHz |
| $f_S$(2) | Sampling rate | - | 0.05 | - | 1 | MHz |
| $f_{TRIG}$(2) | External trigger frequency | $f_{ADC}$=14MHz | - | - | 823 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| $V_{AIN}$(3) | Conversion voltage range | - | 0 ($V_{SSA}$ or $V_{REF-}$ tied to ground) | - | $V_{REF+}$ | V |
| $R_{AIN}$(2) | External input impedance | | - | - | 50 | kΩ |
| $R_{ADC}$(2) | Sampling switch resistance | | - | - | 1 | kΩ |
| $C_{ADC}$(2) | Internal sample and hold capacitor | | | | 8 | pF |
| $t_{CAL}$(2) | Calibration time | $f_{ADC}$=14MHz | 5.9 | | | μs |
| | | | 83 | | | $1/f_{ADC}$ |
| $t_{lat}$(2) | Injection trigger conversion latency | $f_{ADC}$=14MHz | | | 0.214 | μs |
| | | | | | 3(4) | $1/f_{ADC}$ |
| $t_{latr}$(2) | Regular trigger conversion latency | $f_{ADC}$=14MHz | | | 0.143 | μs |
| | | | | | 2(4) | $1/f_{ADC}$ |
| $t_S$(2) | Sampling time | $f_{ADC}$=14MHz | 0.107 | | 17.1 | μs |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$(2) | Power-up time | | 0 | 0 | 1 | μs |
| $t_{CONV}$(2) | Total conversion time (including sampling time) | $f_{ADC}$=14MHz | 1 | | 18 | μs |
| | | | 14 to 252 ($t_S$ for sampling + 12.5 for successive approximation) | | | $1/f_{ADC}$ |

1. Guaranteed by characterization, not tested in production.

2. Guaranteed by design, not tested in production.

3. In QFN36, LQFP48 and LQFP64 packages, $V_{REF+}$ is internally connected to $V_{DDA}$ and $V_{REF-}$ is internally connected to $V_{SSA}$. See Table 2.

4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in Table 43.

## Equation 1: $R_{AIN}$ max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The above formula (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 LSB. Here N = 12 (from 12-bit resolution).

Table 44 $R_{AIN}$ max for $f_{ADC}$ = 14 MHz(1)

| $T_S$ (cycles) | $t_S$(μs) | $R_{AIN}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |

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| | | |
|---|---|---|
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | - |
| 239.5 | 17.1 | - |

1. Guaranteed by design, not tested in production.

Table 45 ADC accuracy - limited test conditions(1)(2)

| Symbol | Parameter | Test conditions | Typ | Max(3) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 56 MHz<br>$f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ,<br>$V_{DDA}$ = 3 to 3.6 V, $T_A$ = 25 °C.<br>Measurements made after ADC calibration | ±1.3 | ±2 | LSB |
| EO | Offset error | | ±1 | ±1.5 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±1.195 | ±1 | |
| EL | Integral linearity error | | ±2.491 | ±1.5 | |

1. ADC DC accuracy values are measured after internal calibration.

2. ADC accuracy vs. negative injection current: injecting a negative current on any standard analog input pin must be avoided, as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 5.3.12 does not affect the ADC accuracy.

3. Guaranteed by characterization, not tested in production.

Table 46 ADC accuracy(1)(2)(3)

| Symbol | Parameter | Test conditions | Typ | Max(3) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 56 MHz<br>$f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ,<br>$V_{DDA}$ = 2.4~3.6V<br>Measurements made after ADC calibration | ±2 | ±5 | LSB |
| EO | Offset error | | ±1.5 | ±2.5 | |
| EG | Gain error | | ±1.5 | ±3 | |
| ED | Differential linearity error | | ±1.195 | ±2 | |
| EL | Integral linearity error | | ±2.491 | ±3 | |

1. ADC DC accuracy values are measured after internal calibration.

2. Better performance could be achieved in restricted $V_{DD}$, frequency, $V_{REF}$ and temperature ranges.

3. ADC accuracy vs. negative injection current: injecting a negative current on any standard analog input pin must be avoided, as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in Section 5.3.12 does not affect the ADC accuracy.

4. Guaranteed by characterization, not tested in production.

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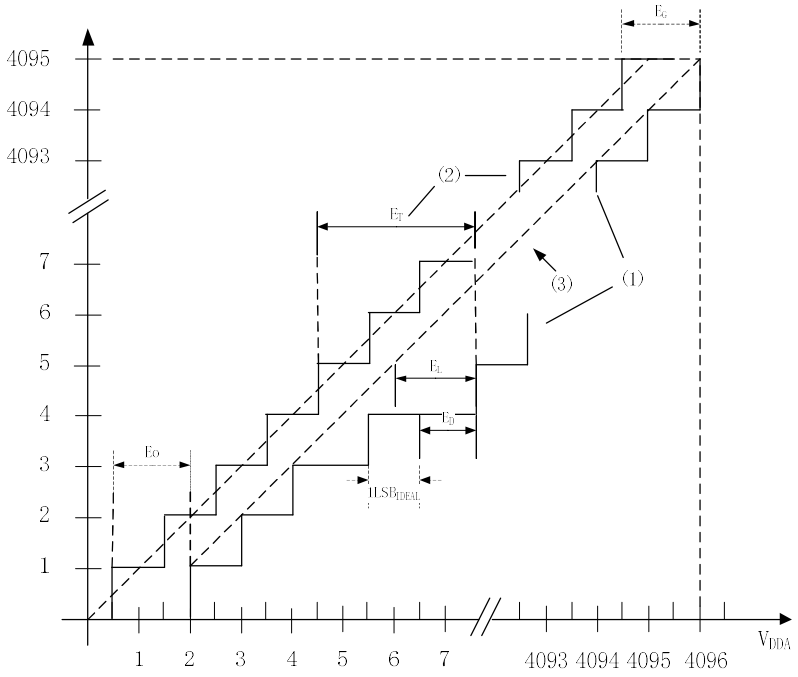


Figure 24 ADC accuracy characteristics

(1) Example of an actual transfer curve

(2) Ideal transfer curve

(3) End-point correlation line

$E_T$ = Total unadjusted error: maximum deviation between the actual and the ideal transfer curves.

$E_O$ = Offset error: deviation between the first actual transition and the first ideal one.

$E_G$ = Gain error: deviation between the last ideal transition and the last actual one.

$E_D$ = Differential linearity error: maximum deviation between actual steps and the ideal one (1 LSB). Here 1 $LSB_{IDEAL}$ = $V_{REF+}$/4096 (or $V_{DDA}$/4096, depending on package).

$E_L$ = Integral linearity error: maximum deviation between any actual transition and the end-point correlation line.

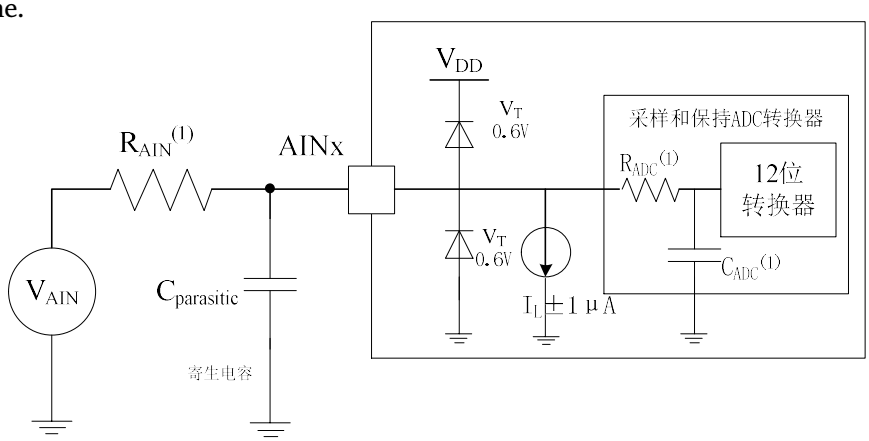


Figure 25 Typical connection diagram using the ADC

1. Refer to Table 46 for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.

2. Cparasitic represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high Cparasitic value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## PCB design guidelines

Power supply decoupling should be performed as shown in the figures, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors must be ceramic (good quality) and placed as close as possible to the MCU chip.

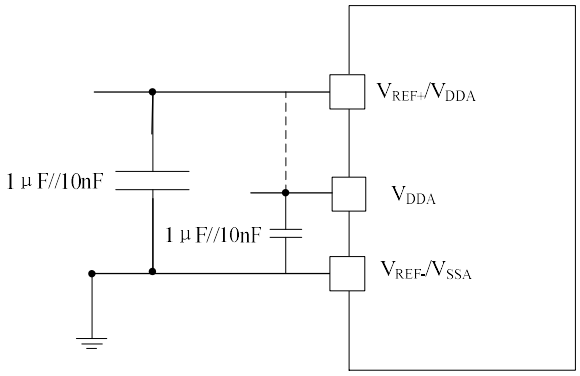


Figure 26 Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)

1. $V_{REF+}$ and $V_{REF-}$ inputs are available only on 100-pin packages.

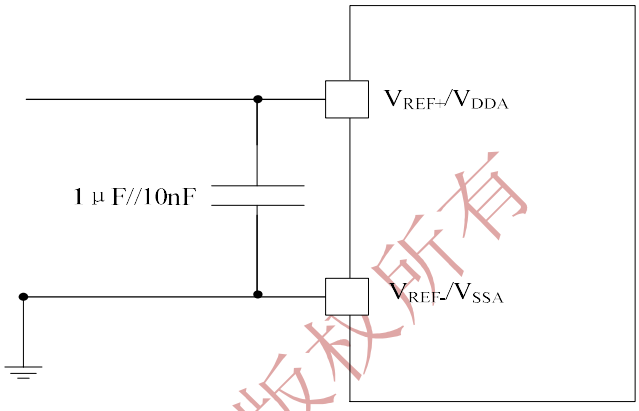


Figure 27 Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$)

1. $V_{REF+}$ and $V_{REF-}$ inputs are available only on 100-pin packages.

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## 5.3.18 Temperature sensor characteristics

Table 47 Temperature sensor characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | | ±1 | ±2 | ºC |
| Avg_Slope(1) | Average slope | 4.0 | 4.3 | 4.6 | mV/ºC |
| $V_{25}$(1) | Voltage at 25ºC | 1.551 | 1.596 | 1.650 | V |
| $t_{START}$(2) | Startup time | 4 | | 10 | µs |
| $T_{S_temp}$(2)(3) | ADC sampling time when reading the temperature | | | 17.1 | µs |

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. The shortest sampling time can be determined in the application by multiple iterations.

# 6. Package Characteristics

## 6.1 Package mechanical data

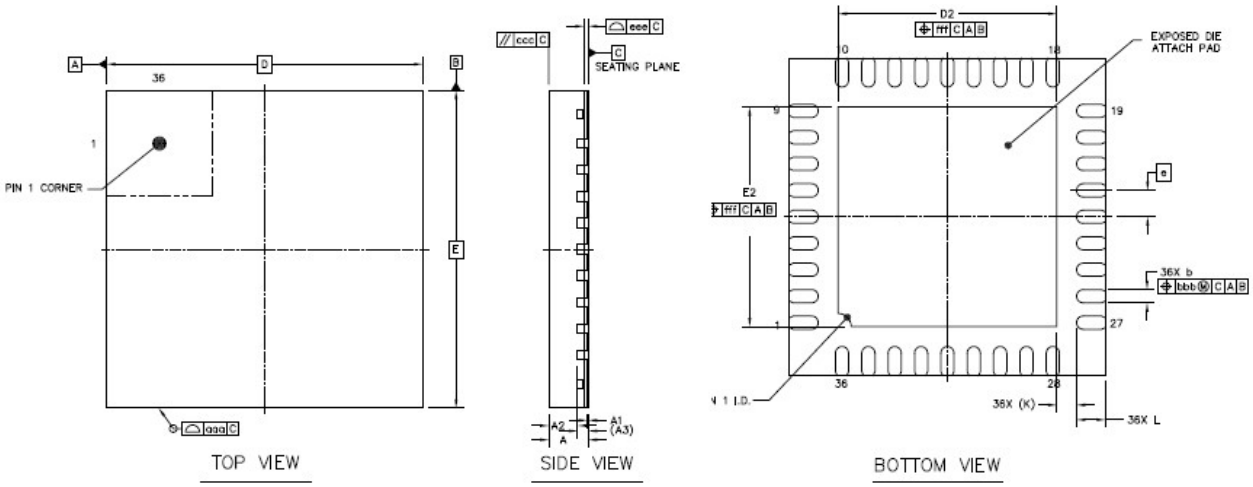


Figure 28 QFN36 package outline

Table 48 QFN36 package mechanical data

| Symbol | millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | 0.203 REF | | |
| b | 0.20 | 0.25 | 0.30 |
| D | 6 BSC | | |
| E | 6 BSC | | |
| e | 0.5 BSC | | |
| D2 | 4.05 | 4.15 | 4.25 |
| E2 | 4.05 | 4.15 | 4.25 |
| K | 0.375 REF | | |
| L | 0.45 | 0.55 | 0.65 |
| aaa | 0.1 | | |
| ccc | 0.1 | | |
| eee | 0.08 | | |
| bbb | 0.1 | | |
| fff | 0.1 | | |

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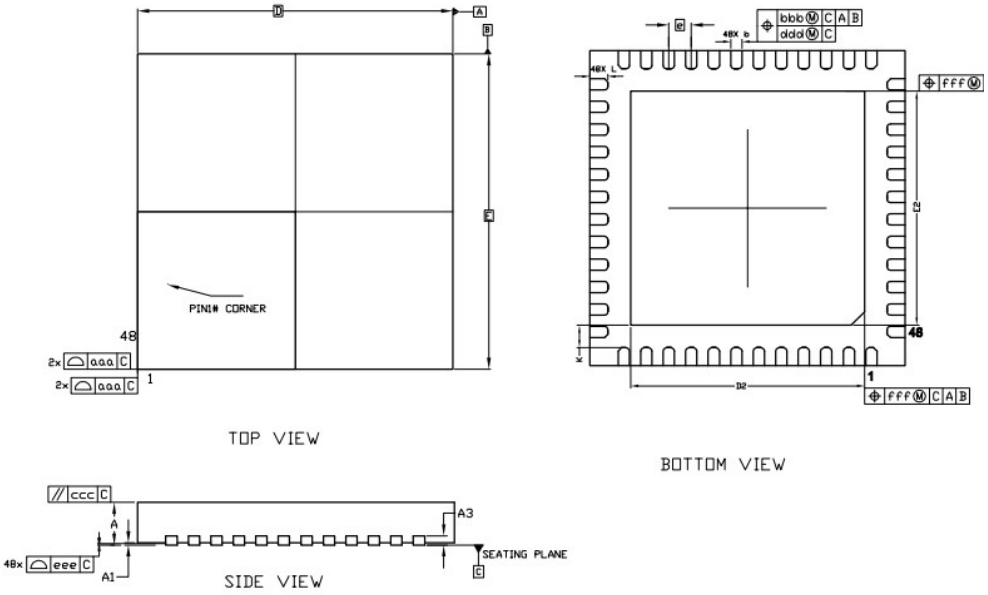


Figure 29 QFN48 package outline

Table 49 QFN48 package mechanical data

| Symbol | millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | - | 0.20REF | - |
| b | 0.20 | 0.25 | 0.30 |
| D | 7.00BSC | | |
| E | 7.00BSC | | |
| D2 | 5.10 | 5.20 | 5.30 |
| E2 | 5.10 | 5.20 | 5.30 |
| e | 0.50BSC | | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.50 | - | - |
| aaa | 0.15 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

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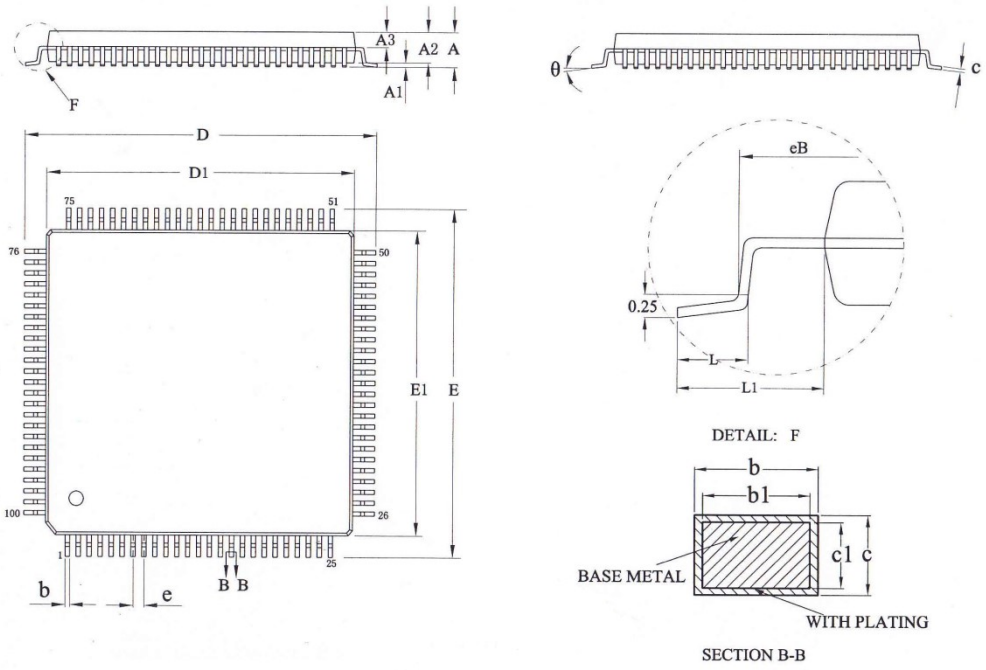


Figure 30 LQFP100, 100-pin low-profile quad flat package outline

Table 50 LQFP100, 100-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | | | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.14 |
| D | 15.80 | 16.00 | 16.20 |
| D1 | 13.90 | 14.00 | 14.10 |
| E | 15.80 | 16.00 | 16.20 |
| E1 | 13.90 | 14.00 | 14.20 |
| eB | 15.05 | - | 15.35 |
| e | 0.50BSC | | |
| L | 0.45 | - | 0.75 |
| L1 | 1.00REF | | |
| θ | 0 | - | 7° |

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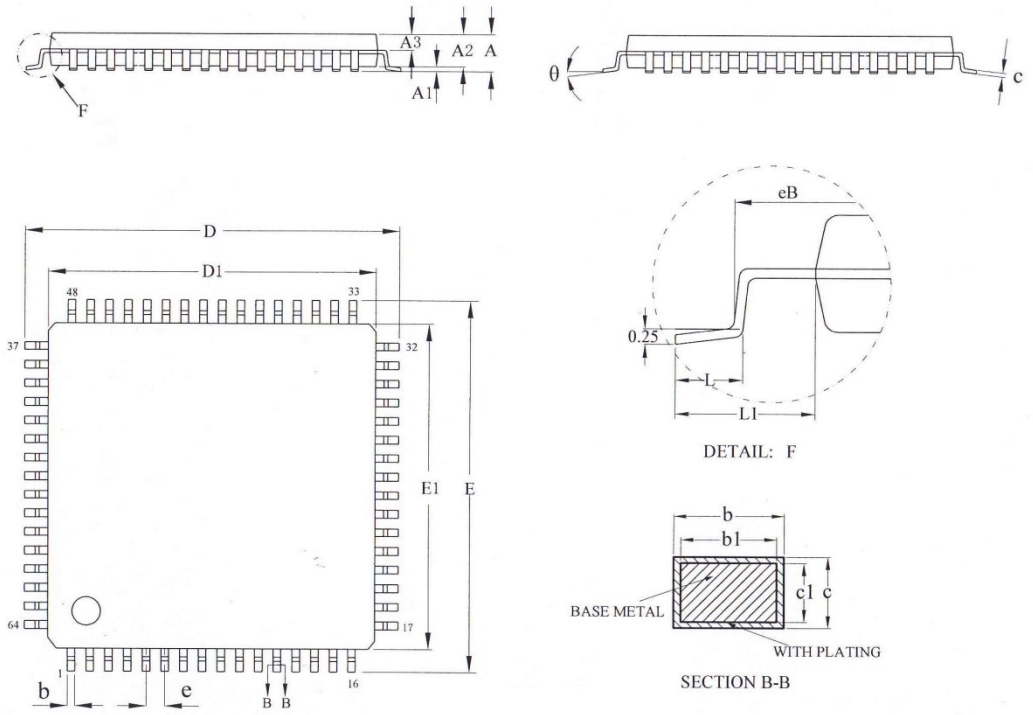


Figure 31 LQFP64, 64-pin low-profile quad flat package outline

Table 51 LQFP64, 64-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.17 |
| D | 11.80 | 12.00 | 12.20 |
| D1 | 9.90 | 10.00 | 10.10 |
| E | 11.80 | 12.00 | 12.20 |
| eB | 11.25 | - | 11.45 |
| E1 | 9.90 | 10.00 | 10.10 |
| e | 0.50BSC | | |
| θ | 0° | - | 7° |
| L | 0.45 | - | 0.75 |
| L1 | 1.00REF | | |

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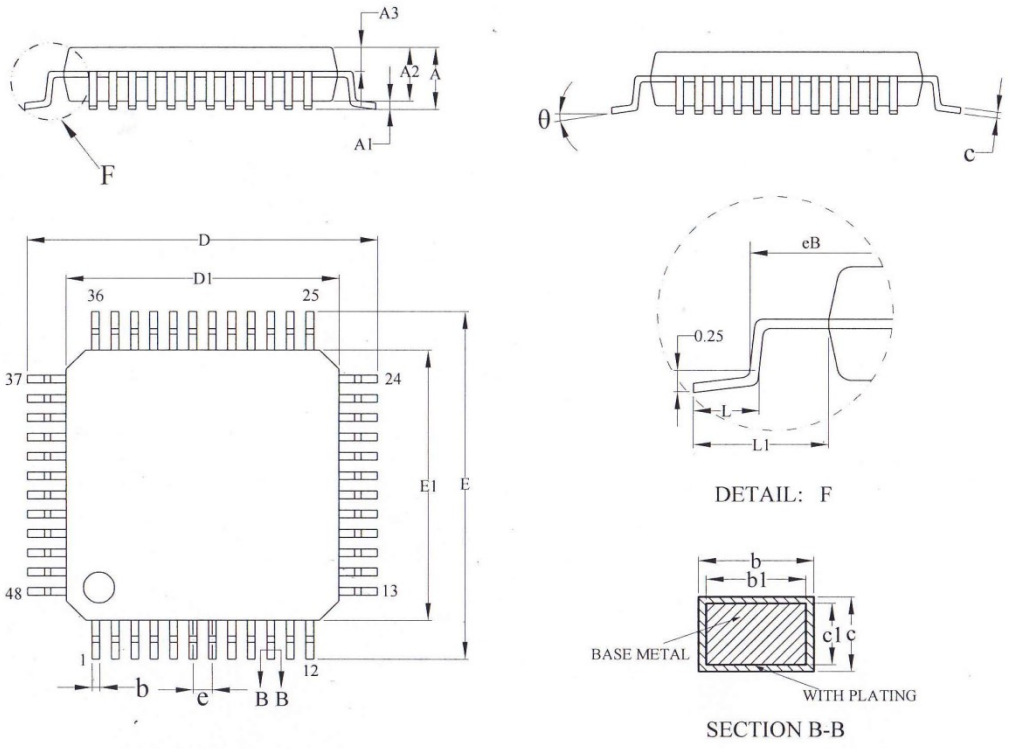


Figure 32 LQFP48, 48-pin low-profile quad flat package outline

Table 52 LQFP48, 48-pin low-profile quad flat package mechanical data

| Symbol | millimeters | | |
|---|---|---|---|
| | Min | Typ | Max |
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| A3 | 0.59 | 0.64 | 0.69 |
| b | 0.18 | - | 0.26 |
| b1 | 0.17 | 0.20 | 0.23 |
| c | 0.13 | - | 0.17 |
| c1 | 0.12 | 0.13 | 0.14 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.20 |
| eB | 8.10 | - | 8.25 |
| e | 0.50BSC | | |
| L | 0.40 | - | 0.65 |
| L1 | 1.00REF | | |
| θ | 0 | - | 7° |

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## 6.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in Table 6.

The maximum chip junction temperature, $T_J$max, in degrees Celsius, may be calculated using the following equation:

$$T_J\text{max} = T_A\text{max} + ( P_D\text{max} \times \Theta_{JA})$$

Where:

- $T_A$max is the maximum ambient temperature in ˚C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in ˚C/W,
- $P_D$max is the sum of $P_{INT}$max and $P_{I/O}$max ($P_D$max = $P_{INT}$max + $P_{I/O}$max),
- $P_{INT}$max is the product of $I_{DD}$ and $V_{DD}$, expressed in watts. This is the maximum chip internal power.

$P_{I/O}$max represents the maximum power dissipation on output pins, where:

$$P_{I/O}\text{max} = \Sigma(V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual $V_{OL}/I_{OL}$ and $V_{OH}/I_{OH}$ of the I/Os at low and high level in the application.

Table 53 Package thermal characteristics

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient — LQFP100 - 14 × 14 mm / 0.5 mm pitch | 46 | °C / W |
| | Thermal resistance junction-ambient — LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | |
| | Thermal resistance junction-ambient — LQFP48 - 7 × 7 mm / 0.5 mm pitch | 55 | |
| | Thermal resistance junction-ambient — QFN36 - 6 × 6 mm / 0.5 mm pitch | 18 | |
| | Thermal resistance junction-ambient — QFN48 - 7 × 7 mm / 0.5 mm pitch | 55 | |

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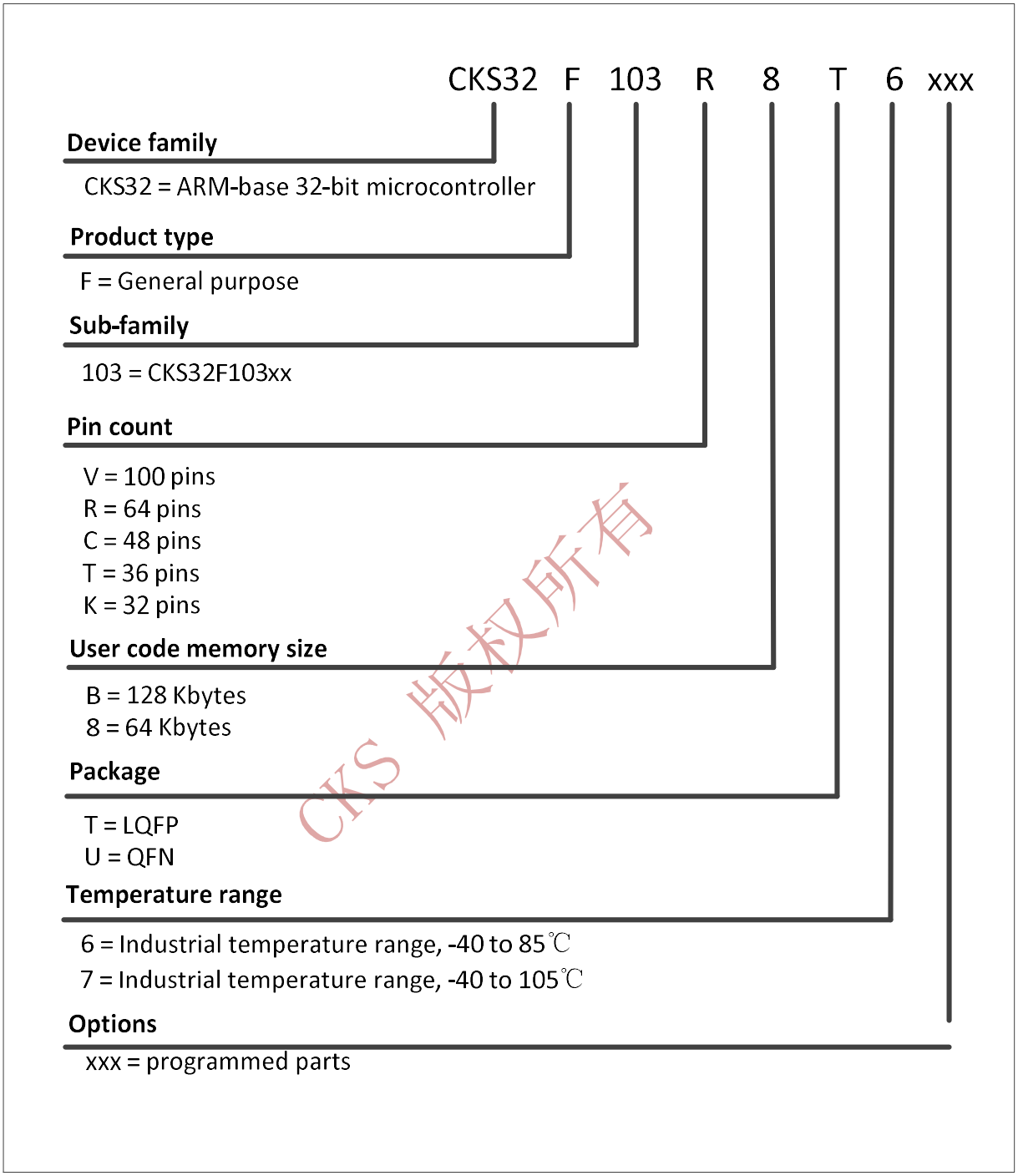
### 6.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.

# 7. Part Numbering

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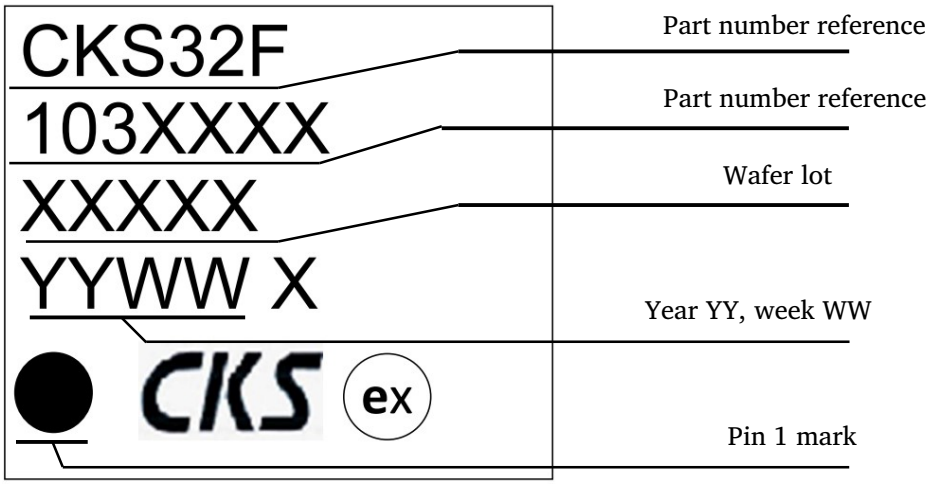
# 8. Product Marking




Note: 1. Font: Arial;

2. Unit: mm;

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# 9. Revision History

| Date | Version | Changes |
|---|---|---|
| 2018.01.18 | Initial draft | |
| 2018.04.20 | 1.0 | Modified the pin definitions of pins 80 and 81 in Figure 3;<br>Added typical values at 48 MHz clock in Table 14; |
| 2018.08.11 | 1.1 | Added Table 15, typical current consumption in Run mode, code with data processing running from internal RAM;<br>Modified typical values at 72 MHz clock in Table 16; |
| 2018.10.10 | 1.2 | Modified the maximum value of fLSE_ext in Table 18;<br>Changed the IDD unit in Table 26 from μA to mA;<br>Modified the min, typical and max values of $V_{25}$ in Table 47. |
| 2018.10.15 | 1.3 | Added Device Comparison / Ordering Information / Part Numbering sections |
| 2020.03.17 | 1.4 | Added QFN36 package content |
| 2020.07.11 | 1.5 | Following modifications based on information from the test department:<br>1. Maximum $I_{DD}$ at 85°C, 8 MHz in Table 12;<br>2. Typical values at 3.6 V in Stop and Standby modes in Table 13;<br>3. Typical $I_{DD}$ with all peripherals enabled in Table 16;<br>4. Max and min HSE frequency in Table 18;<br>5. Max and min LSE frequency in Table 19;<br>6. Max and min HSI frequency in Table 22;<br>7. Max and min LSI frequency in Table 23;<br>8. Max and min PLL input clock in Table 25;<br>9. Typical values of ED and EL in Tables 45 and 46;<br>10. Max, min and typical values of $V_{25}$ in Table 47 |
| 2020.12.30 | 1.6 | Added product marking description |
| 2021.05.08 | 1.7 | Modified PB14 content in Table 2 |
| 2022.05.31 | 1.8 | Modified product temperature range |
| 2022.08.30 | 1.9 | Supplemented data in Section 2.1.17 |
| 2023.05.10 | 1.10 | Modified ordering information |
| 2023.09.27 | 1.11 | Modified typical IDD in Table 13 |
| 2023.11.17 | 1.12 | Modified Flash electrical parameters |
| 2024.01.03 | 1.13 | Added ambient and junction temperature for products with suffix 7 |
| 2024.05.15 | 1.14 | Modified the device comparison table |
| 2025.05.26 | 1.15 | Added QFN48 package content |

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# 10. Disclaimer

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